Honeywell
Honeywell Information Systems Italia

DSS 157 - SUBSYSTEM

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VOLUME 5

This volume is applicable for those products having the following product codes:

- 0896484 R - 0896483 U

Binder 2", 3 rings

Window

T.o.C.		4.819.2.006.1
Description:		
1 PDS DSS 157		78A103839
2 PDS DSC 157		78A103838
3 PDS ALI 130 B		78A104419
Installation DSC 157		4.819.0.001./A
Maintenance DSC 157		4.813.4.001./A
Maintenance schedule type F	DSU167 (ADU157)	4.014.4.645./A
Maintenance schedule type H		4.010.4.646./A
Lubrication Plane		4.014.4.639./A
Preventive Maintenance Log		4.033.4.081./A
Maintenance schedule type F	DSU157D	4.014.4.674./A
Maintenance schedule type H		4.014.4.675./A
Lubrication Plane		4.014.4.676./A
Preventive Maintenance Log		4.033.4.207./A
Parts DSC 157		4.813.5.001.

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SOTTOSISTEMA DSS 157

INDICE DEL VOLUME 5

Questo volume è valido per i prodotti aventi i seguenti codici:

- 0896484 R - 0896483 U

Raccoglitore da 2" a 3 anelli		
Finestra		
Indice		4.819.2.006. 1
Descrizione:		
1 PDS DSS 157		78A103606
2 PDS DSC 157		78A103605
3 PDS ALI 130 B		78A104418
Installazione DSS 157		4.819.0.001.
Manutenzione:		
1 DSC 157		4.813.4.001.
2 DSU 167		4.813.4.201.
Scheda di Manutenzione tipo F	DSU167 (ADU 157)	4.014.4.645.
Scheda di Manutenzione tipo H		4.014.4.646.
Piano di Lubrificazione		4.014.4.639.
Piano di Manutenzione		4.033.4.081.
Scheda di Manutenzione tipo F	DSU157 D	4.014.4.674.
Scheda di Manutenzione tipo H		4.014.4.675.
Piano di Lubrificazione		4.014.4.676.
Piano di Manutenzione		4.033.4.207.
Catalogo DSC 157		4.813.5.001.

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DESCRIPTION

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1.0. GENERAL CHARACTERISTICS

1.1. Introduction

The DSS 157 is a peripheral subsystem with large capacity random access memory, and it consists of a physical unit DSC 157 (refer to DPS No. 78A103605) and of 203 tracks magnetic disk handler DSU 167 (refer to DPS No. M50EB00281), or DSU157D disk handler (refer to SSP No.0157-00-00).
The memory medium consist of interchangeable packs with 11 disks, with 20 useful surfaces.
The subsystem consist of a controller to wich in the maximum configuration we can connect 3 cluster DSU167, of 3 drivers each one or 9 DSU157D, of wich eight on line and one of spare.

1.2. General

1.2.1. Funcional characteristics

- The data are written serially, in "sector" mode, either in 6-bit alphanumeric characters or in 8-bit characters.
- Every unit has a 20 arm read and write device; each arm has a read/write head and it is inserted between the facing surfaces of the disks. The heads are of the floating type (not contact head).
- The average time for the head positioning on one track is 87 msec. (min. 25 msec. maximum 135 msec); it is possible to overlap completely the positioning operations related to several units of the subsystem.
- The average latency time is 12.5 msec (minimum 0 msec, maximum 25 msec.).
- The characters transfer speed is 208,000 chrt/sec. in 6-bit mode, 156,000 chrt/sec. in 8-bit mode.
- The write method is "double frequency NRZ1".
- The subsystem, that we can connect to the C.P.U. GE 120 and GE 130, in the transfers of data needs the maximum priority.

1.2.2. Medium used

The medium used to write information consists of a disk pack which may be assembled and removed very easily on the rotating mechanism of the single units. The discpack is of type IBM 2316 and it consists of 11 disks with a 14" diameter, assembled on the same axis and with a 0.4" space between one another.

The disck pack used in the DSU167 and in the DSU157D is recorded into a six tracks shifted area comparison to the used area by to I.B.M. 2316.

The two external surfaces are not used to contain information, the remaining 20 surfaces are coated with magnetic oxide and the 20 read/write heads which are inserted by two, between adjacent disks, go near them.
On the lower part it is integral with a metallic disk, having on the outside ring a slot indicating track beginning (index mark).
This slot is felt by a sensing element assembled on the unit.
The disk pack, during unit performance, rotates at the speed of 2,400 r.p.m.

1.2.3. Medium format

The disk pack format is the following :

- the circle described by a head on the corresponding face of the rotating disk is called track;
- the assembly of the 20 tracks on which the 20 heads run simultaneously is called cylinder;
- every track is in addition divided in 10 zones called sectors.
  There are therefore, in a disk pack :
  10 secotrs per track (0 - 9)
  20 tracks per cylinder (0 - 19)
  203 cylinders per pack (0 - 202)
- Some of these cylinders (3 [illegible] average) will be kept as a reserve to write the information which cannot be written on the tracks of the remaining cylinders which will therefore result as being faulty.
  The nominal capacity of the medium will therecore be referred to 200 cylinders only.

- The 40, 600 sectors per pack are normally identified with a number ranging from 0 and 40,599.
  This number is the address of the sector and is written in the sector itself in the area called header.
- The sector addresses are increasing from the top (face 0) to the botton (face 19), within a cylinder and from the outside (cylinder 0) towards the inside (cylinder 202) within a pack.
  The controller included an option that limits the useful cylinders to 100 (00 + 99) + 3 of spare (200 + 202).

1.2.4. Medium capacity

Sector mode	6-bit chrts.	8-bit chrts.
Sector	384	288
Track	3,340	2,288
Cylinder	76.800	57.600
Pack	15.360.000	11.520.000
On-line max. capacity	122.680.000	92.160.000

1.2.5. Compatibility

The DSS 157 for the 100 line is compatible, as far as the format of the information recorded on disc are concerned with the equivalent subsystem connecting the disc handler 167 to the 400/600 line.
It is therefore possible an exhange of the recorded supports taking into account that a transcoding from software will be necessary.
No compatibility restriction exists, within the DSS167, between the disks recorded on DSU 167 and DSU 157D

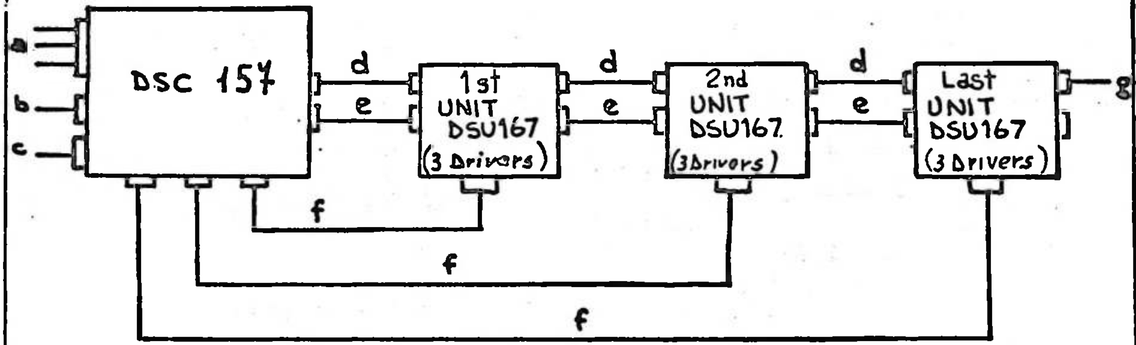
1.3. Physical configuration

The subsystem may have a minimum configuration consisting of one physical unit DSC 157 and one cluster with three drivers DSU 167 or three DSU 157 D and a maximum configuration of one physical unit DSC 157 and three clusters with nine drivers or nine DSU 157 D of wich eight on line and one of spare. In addition, the lay-out may have either floor plates or double floor.

- Refer drawing N° 78B103865 for subsystem with DSU 167
- Refer drawing N° B78106931 for subsystem with DSU 157 D

1.4. Electric configuration

The subsystem electric configuration with DSU 167 is given in in the figure below:


a
b
c
DSC 157
d
e
1st UNIT DSU167 (3 Drivers)
d
e
2nd UNIT DSU167 (3Drivers)
d
e
Last UNIT DSU167 (3 Drivers)
g
f
f
f

a - logic interface
b - external d.c. voltage (+20)
c - a.c. voltage
d - a.c. voltage
e - multiplex cables
f - simplex cables (1 for each spindle)
g - terminator

1.4.1. Signals distribution

The subsystem is connected to CPU by means of 3 cables which start from the DSC 157 and allow the exchange of the various logic signals of the 100 interface described on P.P.S. No. 300740110.
Within the subsystem the various units are connected one another and to the DSC 157 by means of simplex and multiplex cables.

1.4.2. D.C. Voltages

The subsystem takes from the system central power supply a +20V voltage to supply some circuits of the controller.
A power supply internal to the DSC 157 supplies the stabilized d.c. voltages necessary to the controller logic and, par

tly, those used by the various disk handlers as the remaining ones are generated by a power supply located internally to every disk handler.

1.4.3. A.C. Voltages

The a.c. voltage needed by the subsystem is the following:

220V ± 10% - three phases + ground
50 Hz ± 1/2 Hz
} ALI 260 Model D

208V ± 10%
60 Hz ± 1/2 Hz - three phases + ground
} ALI 260 Model P

The DSC 157 includes an a.c.distribution panel (ALI 260), connected to the subsystem to which the units are bus-connected. The maximum absorbed current is 24 A.
In addition, both the controller ventilation group (VAR 585) and the ALI 130Bpower supply are connected with the ALI 260.

1.5. Mechanical configuration

The Physical Units forming the subsystem have the following sizes (in millimeters):

	DSC 157	DSU 167	DSU 157 D
height	980	965	1003
depth	704	830	838
length	980	1810	635

The subsystem sizes in the version with floor plates, are defined by the assembly of the controller, floor plates (mm. 840), number of disc handlers connected; in the version with double floor, the sizes cannot be defined as the physical lay-out may be different and is limited only by the cables length.

2. REQUIRED ENVIRONMENT CONDITIONS

For these data refer to what has been given in the PDS of the single "physical units".

3. OPTIONS LIST

For these data refer to what has been given in the PDS of the single "physical units".

4. GENERAL PROGRAMMING CHARACTERISTICS

The functions which can be realized by the subsystem and the description of the various commands it may receive are given in the PDS of the DSC 157 physical unit No. 78A103605.

5. OPERATING AND MAINTENANCE CHARACTERISTICS

5.1. Operating panel (DSU 167)

The subsystem has not its own panel.
The subsystem operation status is signaled by the ligh indicators present on the command panel of the single units.
The panel includes also the push-buttons which serve to handle the machine.
The ligh indicators may be incorporated or not in the push-bottons.

- START/STOP push-botton

The START/STOP push-button allows the powering on of the unit motor, when the power supply is on and the disc has been inserted on the unit and the cover has been closed. When the push-botton is on the START position, the motor of the disc unit is energized, the neads are loaded and the head carriage is positioned on cylinder zero; when it is in the STOP position, the unit motor is off, the heads are unloaded and the carriage has been removed from the dispack.

- Unit status indicators (FILE READY - FILE ALERT).
  When the START/STOP push-button is in START position the "File Ready" indicator becomes green after the following two events have occurred : the heads have been loaded, the heads carriage is positioned on the cylinder zero. This indicator stays green until the START/STOP push-button is not set in STOP position or there is a power supply failure. The "File Alert" indicator becomes red every time the unit protection circuits detect a malfunction or directly for a command from program (operator call). Such a signal may be eliminated : removing the reasons which have caused the intervention of the check circuits, by pressing the status indicator and setting the START/STOP in STOP position.
- Identifier of the unit physical number. Each unit includes a plug usable by the user, which allows to identify with a number variable from 0-7 every single unit.
  The ninth unit is a spare one and it identified by a special plug (Plug "SP" for DSU167 and plug "S" for DSU157D)
  Within the subsystem there may be no units without plug.
  The absence of the plug corresponds: to the plug with code zero for the DSU167 and to the plug with code "S" for the DSU157D.
  The name of the unit may be changed only when the subsystem is stopped.

5.2. Maintenance panel

The subsystem does not have a maintenance panel _
For maintenance off-line, the DSU167 may use a Suitcase-tester and the DSU157D have an internal maintenance panel _

5.3. Failures diagnosis

For failures trouble-shooting during a first phase the special diagnostic programs are used and during a second phase the diagnostic equipment VAR 583 described in drawing No. 14623102 is used. The diagnostic programs used are described in drawing No. 3T479 1200H

5.4. Alert conditions

The controller ventilation group has a protection device for no ventilation whose intervention causes the complete switching off of the system.

6.0. OPERATIONS THEORY

The logic view of the subsystem must be divided in the various component physical units.

6.1. Power supplies, performance and distributions sequences

In order to switch the subsystem on, the breaker set on the ALI 260 of the DSC 157 must be set on ON, supplying then the a.c. to the power supply (ALI 130B) and to the blowers (VAR 585); at this point it is possible to switch the whole system on.
The procedure to power on the various units is the following:

- check that the interested units have the local breaker "on";
- supply the d.c. voltages to the system acting on the CPU panel; at this point the ALI 130B is in condition to be turned on and to enable the ALI 260 to supply the a.c. voltage to the various units;
- press the START push-button on the interested units.

7.0. TEST PROCEDURE

Prepare a subsystem with the various physical units already tested and check their performance with the diagnostic programs.

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1. GENERAL DESCRIPTION

1.1. Foreword

It is a random access memory peripheral subsystem.The memory support consists of interchangeable packs with 11 discs and 20 useful surfaces.
The subsystem consists of a controller to which to connect to the maximum 3 clusters with three drivers,each one with eigth on-lines and a spare one.
The subsystem will be connectable to the GE 120 and GE.130 Central Processors either directly to a standard Central Unit or after a Multiperipheral Adapter.

1.2. General

The disc units are of the DSU 167 type developed by IDD in Oklahoma,or DSU 157 D type developed by Honeywell in Lawrance

1.2.1. Performances

- The write method is "Double frequency NRZ1".
- The characters transfer speed is :

  208,000 chrt/sec. in 6 bit mode
  156,000 chrt/sec. in 8 bit mode.

- The data are written serially in "sector"mode either al alphanumerical characters of 6 bits each, or as 8 bit characters.
- The capacity of a disc pack is :

  15,360,000 6-bit characters
  11,520,000 8-bit characters

- The average access time on a track is of 87 msec.(min.25 msec., max.135 msec.);it is possible to overlap completely the positioning operations interesting several units of the subsystem.
- The average latency time is 12.5 msec.(min.0 msec.,max.25 msec.).

1.2.2. Compatibility

The DSC157 is compatible with the DSC 167(controller for disk sub system connectable to GE 400/600).
Compatibility means that it is possible to exchange the media written by the two systems.
It is necessary a software decode .

1.3. Physical configuration

The DSC 157, as indicated by the drawing No. 78B103732 consists of the following parts:

- Controller	GUD 040
- Power supply	ALI 130B
- A.C. distribution module	ALI 260
- Exchange board	VAR 586
- Ventilation module	VAR 585
- Cabinet	CON 340

1.3.1. Controller

The controller consists of the logic circuits which provide to the exchange of data and commands between the C.P.U. and the disk handler.
It is realized according to TTL and DTL micrologic standard (refer to specs. No. 30074082) and uses the following types of integrated circuits:

TEXAS	SGS	CONFIGURATION	ELEMENT PER PACKAGE	TYPE
SN7400N	9002	NAND with 2 inputs	4	TTL
SN7410N	9003	NAND with 3 inputs	3	TTL
SN7420N	9004	NAND with 4 inputs	2	TTL
SN7430N	9007	NAND with 8 inputs	1	TTL
SN7451N	9005	NAOR with 4 inputs	2	TTL
SN15848N	94859	FF J.K. Mast. Slave	1	DTL

Physically it is contained in two standard SMN modules and it consists of 159 boards of 52 different types.

1.3.2. Power supply

The power supply gives the d.c. stabilized voltages necessary to the controller logic, to the circuits of interface with the disk handler and to the disk handler itself.

The generated voltages are:

Voltage	Max. current	Use
- 36 V	2,05 A	DSU
- 3 V	8,24 A	GUD 040 - DSU
+ 3 V	3,22 A	DSU
+ 5 V	12 A	GUD 040
+ 5 V	15,52 A	DSU

The +20V voltage for the interface circuits an for the GUD 040 is supplied by the connected C.P.U.

1.3.3. A.C. distribution module

It provides to the a.c. voltage distribution necessary both for the DSC 157 and the connected disk handlers.
The maximum current which can be given is equal to 24A.
There are two models:

a - Model D 220 V 50 Hz
b - Model P 208 V 60 Hz

The difference between D and P models consists of the application of different types of a.c. relay.

1.3.4. Exchange board

It is the element multiplying the simplex cables towards the connected disk handlers. (9 drivers)

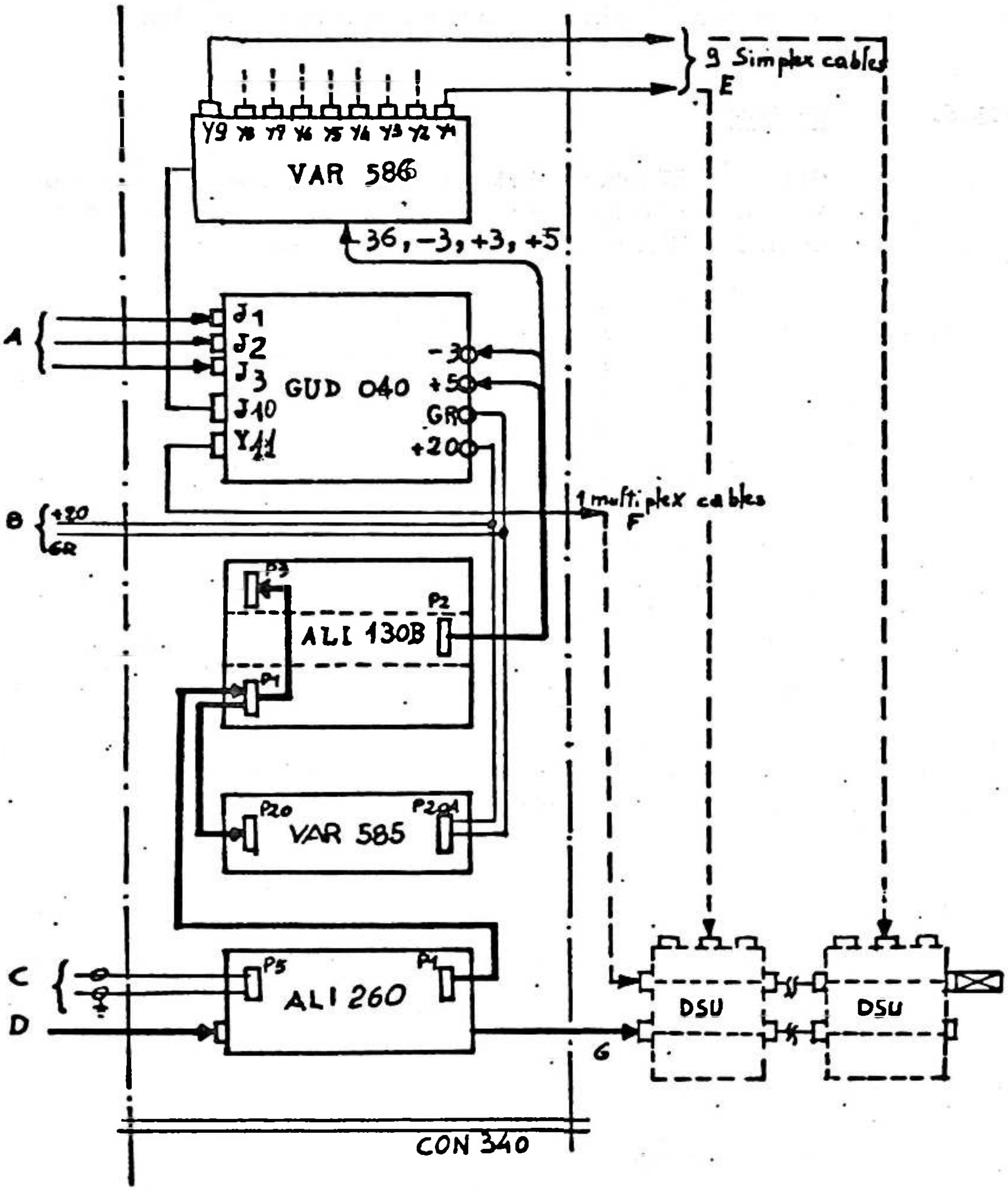
1.3.5. Ventilation board

It provides for the controller logic ventilation.
It is provided with a no ventilation protection.

1.3.6. Cabinet

The DSC 157 cabinet belongs to the free standing type. The access to internal devices is allowed by removable covers on the sides of the cabinet itself.

1.4. Electric configuration



Interface towards C.P.U.:

a = logic interface
b = external D.C. voltage cable (+20 V)
c = a.c. voltage control
d = a.c. voltage

Interface towards DSU:

e = simplex cables
f = multiplex cable
g = a.c. voltage

☒ = terminator plug inserted only on the last unit.

1.4.1. Interface towards C.P.U.

1.4.1.1. Logic interface

The connection between the controller and the C.P.U. is done according to the procedures of the 100 line peripheral interface No. 30074011.
The cables making up the connection are fixed on the controller on connectors J1, J2 and J3 and are made up as per the following table:

CPU SIDE PIN	DSC-J1				DSC-J2				DSC-J3	
	Signal	pin	Signal	pin	Signal	pin	Signal	pin	Signal	pin
1	AIFUT	E	AIFET	U	CAGUT	E	PUOOT	U	AEBET	A
2	BIFUT	F	BIFET	V	FINUT	F	MAPET	V	AECOT	B
3	CIFUT	H	CIFET	W	CONUT	H	TESET	W	FECOT	H
4	DIFUT	J	DIFET	X	VICUT	J	MARET	X	FICOT	J
5	—		—		—		—		—	
6	EIFUT	K	EIFET	Y	FINET	K	MATET	J		
7	FIFUT	L	FIFET	Z	PEOCT	L	INEST	Z		
8	—		—		—		—		—	
9	GIFUT	M	GIFET	AA	SECET	M	CAPET	AA		
10	LIFUT	N	LIFET	BB	FISET	N	Z106T	BB		
11	—		—		—		—		—	
12	MIFUT	P	MIFET	CC	SECOT	P	IGOLT	CC		
13	TE1OT	R	TU1OT	DD	EGOLT	R	NU1OT	DD		
14	—		—		—		—			
15	TU2OT	S	TE2OT	EE	ERCAT	S	NU2OT	EE		
16	TE3OT	T	TU3OT	FF	RACUT	T	NU3OT	FF		
17	—		-		—		-		—	

The logic levels on the interface are defined as follows:

- for a signal having a given logic meaning (e.g. FINET), this meaning is verified (e.g. the indication of termination is present) when on the lead corresponding to the signal there is the "Zero Volt" voltage level;

- to the contrary the signal is absent when the lead corresponding to the signal is at positive level "+5". This is valid both for pulse signals and levels.

1.4.1.2. External D.C. voltage cable

It arrives from the C.P.U. +20V power supply and serves both to condition the subsystem power supply (ALI 130B) switching on and to supply some special circuits, the interface circuits with C.P.U. and the write oscillator.

1.4.1.3. A.C. Voltage control

It consists of two cables which make up the connection between the DSC 157 ALI 260 and the other ALI 260 present in the system.
The cables consist each one of two wires plus a shield.

1.4.1.4. A.C. Voltage

The a.c. voltage is supplied to the system through a HUBBEL plug present on the ALI 260.
The needed A.C. power supply is the following:

220 V ± 10%
50 Hz ± 1/2HZ } three-phases + ground – Model D

208 V ± 10%
60 Hz ± 1/2HZ } three-phases + ground – Model P

1.4.2. Interface towards D.S.U.

1.4.2.1. Logic levels

The correspondence between the logic and electric levels of the interface towards the D.S.U. varies depending on the circuit used.
The signals between controller and disk handler are exchanged either along coaxial lines or along twisted lines.

a. Signals exchange on coaxial lines.

It is done through the TASE board if the transmission goes towards the disk handler (WRITE DATA - VR10U ÷ VR18U) and through the RILE board if the transmission arrives from disk handler (READ DATA - LE00U ÷ LE08U). In the first case the correspondence between transmitted logic levels and electric levels is the following:

logic level "0" = electric level +3V
logic level "1" = electric level 0 V

In the second case the correspondence between the received logic levels and electric levels is the following:

logic level "0" = electric level 0V
logic level "1" = electric level +3V

b. Signals exchange on twisted lines.

This function is performed by the TACO (transmiting) and RICO (receiving) boards:
The correspondence between the logic levels in reception and in transmission and the electric ones is the following:

logic level "0" = electric level +1.5V
logic level "1" = electric level -3V

1.4.2.2. Simplex cables

These cables are used to connect the DSC 157 to the various disk handlers according to a star disposition.
On the DSC 157 side they are derived from an exchange board (VAR 586) which to the maximum may have in output 9 connectors all having signals configurations as listed in the table below:

Interface		DSC 157 - Con.Y1-Y9
Pin	Wire name	Signal
1	+ 5 Volts	
2	+ 5 Volts	
3	DC Ground	
4	DC Ground	
5	Write Data (coaxial)	VRIXU (X=0-8)
10	DC Ground	
11	DC Ground	
12	Read Data (coaxial)	LEXXU (XX=00-08)
13	+ 3 Volts	
14	+ 3 Volts	
15	- 36 Volts	
19	- 3 Volts	
20	- 3 Volts	
21	Seek Complete } twisted wire	
26	Ground	
22	Selected Module } twisted wire	
27	Ground	
23	Module Select } twisted wire	
28	Ground	
25	Shield Ground	

1.4.2.3. Multiplex cables

They are used for a bus connection between disk handlers and the DSC 157.
The transmission occurs on twisted type lines.

Honeywell
Honeywell Information Systems Italia

DSC157 PHYSICAL UNIT
P.D.S.

1° APPLIC.

Interface			DSC 161–Conn. Y5
Signal Pin	Ground Pin	Description	Signals
1	2	Drive Bus 0	BUS0U
3	2	Drive Bus 1	BUS1U
4	5	Drive Bus 2	BUS2U
7	5	Drive Bus 3	BUS3U
8	10	Drive Bus 4	BUS4U
11	10	Drive Bus 5	BUS5U
12	13	Drive Bus 6	BUS6U
14	13	Drive Bus 7	BUS7U
15	16	Set difference tag	SEDIU
17	16	Set Cylinder Tag	SECIU
18	20	Set head and Direction Tag	SETIU
21	20	Control Tag	SERIU
22	63	Control Select 0 ✓	UNO0U
23	63	Control Select 1 ✓	UNO1U
24	63	Control Select 2 ✓	UNO2U
40	41	Cylinder Address Register 7	NOT used by controller " " " "
42	41	" " " Reg. 6	" " " "
43	44	" " " " 5	" " " "
45	44	" " " " 4	" " " "
46	47	" " " " 3	" " " "
48	47	" " " " 2	" " " "
49	50	" " " " 1	" " " "
51	50	" " " " 0	" " " "
52	53	Select.drive Ready	REDIU
54	53	Selected On Line	OFLIU
55	56	Selected Index	INDEU
57	56	Selected Drive Uns.	UNSAU
58	59	Select.SeekIncompl.	SEINU
60	59	Select.End of Cylind.	FICIU
62	63	Control Select 3 ✓	UNO3U
64	63	Select.Write Current enable	not used
65	66	Head Extended	EXTEU
78	66	+36V Sequence Power	SEPIC
76		Controlled Ground	GROUND
77		Sequence Pick (in-out)	SEPIC
79		Terminator + 3 VDC	
80		Shield Ground	
82		Shield Ground	

REVISION

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IND. REV.

UNIT

S.T.

COMPIL. G. Ferrari/ob.fb	APPR.	SEZ. SEC. S.P.S.–I.S.I.	N° 78A103838 A
EMISS. MARCH 1971		LOC. Pregnana	FO. 18

Cod. 3096128 F

1.1.2.4. A.C. cable to DSU

The a.c. power is distributed to the subsystem by means of a cable coming out from the ALI 260 of the DSC 157 and bus-connecting the disk handlers.
The voltage so distributed consists of the three-phases and the ground wire.

1.5. Mechanic configuration

The DSC 157 is completely contained in a free standing cabinet.
It is possible to have access to the internal parts opening the covers which close the cabinet along the two longest sides, as the others on the two remaining sides are screwed to the frame.
The sizes of the cabinet complete with covers are the following: 980 x 700 x 980 mm.
Inside the cabinet there are the three groups which form the DSC 157. They are:

- power supply box (ALI 260):
  it may be pulled out removing a block and rotating it towards the outside;
- power supply + exchange board (ALI 1308-VAR 586):
  this group is fixed at the center of the cabinet and consists of 3 SMI modules;
- controller + ventilation group (GUD 040 + VAR 585):
  this group may be pulled out rotating it towards the outside and it consists, in total, of 2 and 1/2 SMI modules.

The DSC 157 physical unit weighs 200 Kg.

2. REQUIRED ENVIRONMENT CONDITIONS

2.1. Operative conditions

The temperature limits are 10° - 38°C equal to 50°-100°F.
The humidity limits are 20-80%.
The atmospheric pressure must be 780 - 585 mm of Hg.

Note: the temperature and humidity rate of change must be such not to cause condensing of vapor on the units.

2.2. Storage and transport conditions

In storage and transport conditions it may undergo temperatures ranging from -29°C to +74°C equal to -20°F to +165°F.

Note: the temperature and humidity rate of change must be such not to cause condensing of vapor on the units.

- For the other requirements refer to "Common Requirements to design GEISI Products" No. 300140030.

3. OPTIONS LIST

An option is planned to limit the number of cylinders from 00 to 99.
The use of the alternative cylinders stays unchanged.

4. GENERAL PROGRAMMING CHARACTERISTICS

4.1. General

4.1.1. Medium format

The medium used to read or write information consists of eleven disks collected in a single cartridge which may be easily assembled on and removed from the transport mechanism of the sirgle units.

The disk cartridge, during the unit performance, rotates at the speed of 2400 rpm.
The disk pack format is the following:

- the circumference described by a head on the corresponding face of the rotating disk is called track;
- the whole of the tracks examined simultaneously by heads is called cylinder;
- every track in addition is divided in 10 zones called sectors.

Therefore there are in a disk pack:

- 10 sectors per track;
- 20 tracks per cylinder

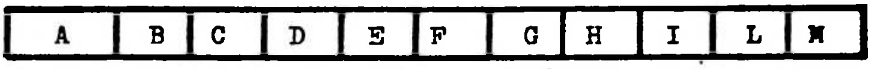
- 203 cylinders per pack.

Some of these cylinders (3 in the average) will be kept as a reserve to write the information which cannot be written on the tracks of the remaining cylinders, which will be marked as faulty.

The medium nominal capacity will therefore be referred to as 200 cylinders only.
The writing method is "double frequency NRZ1".

4.1.2. Track Format (ref. timing 78B103727 page 7)

Every track structure is as follows:



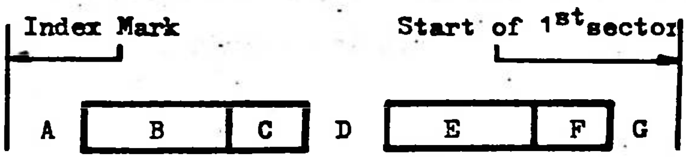
Zone A : Track Header
Zone B – M : sectors (0 – 9)

Every sector may be addressed separately.

4.1.2.1. Track Header format

The Track Header is a special type of information written starting from the index mark (Pulse indicating the track beginning) and before the first sector.
These information are used by the program in case of faulty track, to associate to the faulty track the address of the alternative track.

The Track Header structure is as follows:



Zone A (270 bits) : Gap
Zone B (18 bits) : Home Address
Zone C (12 bits) : Cyclic code related to the home address.
Zone D (144 bits) : Gap
Zone E (18 bits) : Record zero
Zone F (12 bits) : Cyclic code related to Record Zero
Zone G (294 bits) : Gap
+6 8

The useful zones which may be modified by program are the following:

Home Address : it contains all the information which define the track position and precisely:

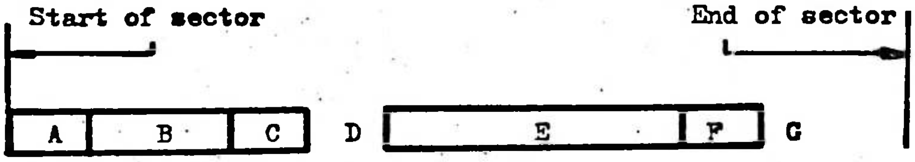
- track indicator (2 bits): it specifies if the track is good, faulty or alternative (i.e. substituting a faulty track);
- cylinder address (8 bits): it indicates in binary code the cylinder address in which the information is recorded; from 000 to 202;
- head name: it indicates in binary code the head name within the cylinder;
- 3 "0" bits.

Record Zero : when the track is good or alternative, it is the same as the Home Address; when the track is faulty, it contains all the information which define the position of the replacing track according to the structure for the Home Address.

4.1.2.2. Sector Format

Every sector includes an area reserved to the prewriting of 3 characters forming the address (header), a zone reserved to data writing and some service zones.

The sector structure is as follows:



768
1190
1951
25040 ≈ 7-10%

Zone A (24 bits) : Address Mark and Data Mark - Service area indicating the header start.

Zone B (19 bits) : Header.

Zone C (12 bits) : Cyclic code - used to detect an error on the header..

Zone D (144 bits) : Data Gap and Data Mark - service zone which precedes the data block.
199

Zone E (2304 bits) : Data block - zone in which the information arriving from CPU are written.

Zone F (12 bits) : Cyclic code - used to detect errors on data

Zone G (318 bits) : Gap - in the case of the last sector this zone has a variable length and ends at the subsequent index; it is denominated as "long gap".

The useful areas which can be modified by program are the following:

Header : it contains the following information:
- track indicator (2 bits): it specifies whether the track is good, faulty or alternative;
- cylinder address (8 bit): it indicates the cylinder address from 000 to 202;
- head address (5 bits): it indicates the head name within the cylinder;
- sector address (4 bits): it indicates the sector address within the track from 0 to 9.

Data block : it contains 384 characters if operating in 6-bit mode or 288 characters if operating in 8-bit mode.

4.1.3. Character format

The data block may be organised in one of the following ways:

a. 6-bit mode: the written character consists of 6 information bits, in order of decreasing weight.

b. 8-bit mode: the written character consists of 8 information bits, in order of decreasing weight.

In both cases the characters are written without check bit. The information check is performed writing at the end of the data zone 12 Cyclic Code bit, which are function of the information previously recorded in the data zone.

In this way it is possible to obtain a better packing of the information and therefore a better media capacity.

The Cyclic Code is generated in a 12-bit shift register, in the following way.
The register is initially reset, then the exclusive OR between each written bit and the most significant bit of the register is performed; the register is shifted(losing the most significant bit) introducing the exclusive OR result in the less significant position of the register.

At the end of the data writing, the complement to the register content is written in decreasing order of weight.

The two writing modes (with 6 and 8 bits) may be present together on the same track, on different sectors.

In addition, a sector written in 6-bit mode may be read in 8-bit mode, reading 3 8-bit characters every 4 6-bit characters written on disk.

This may be used when transfer rate limits forbid the 6-bit mode use.

The inverse operation is also possible, i.e. to read in 6-bit mode a sector written in 8-bit mode, performing afterwards a compression by software in order to obtain the information back to their original form.

In the 6-bit mode data write operation, the controller does not write the two most significant bits i.e. bits GIFUT and LIFUT.

In the 6-bit mode read operation, the controller provides to form again the 8-bit information to be sent to the interface expanding the information in the following way: the first 6 bits (AIFUT - FIFUT) stay unchanged; the 7th bit is equal to the complement of the 6th bit (GIFUT = $\overline{\text{FIFUT}}$) and the 8th bit is equal to the 6th (LIFUT = FIFUT).

4.2. Commands description

4.2.1. General

The controller provides to the performance and the check of the operations issued from the connected CPU, to check the data transfer from and towards the disk unit and to signal the various subsystem states to CPU.

The commands may be divided in:

a) commands which do not occupy the controller:

- general reset;
- operator call;
- positioning;
- addressing;

b) commands which occupy the controller:

- return to home;
- write
- read
- check.

The command of Return to Home occupies the controller only for a time which is less than 3 μsec, after which the operation continues off-line from the unit.

c) specific commands for diagnostic hardware:

- selector advance.

4.2.2. Commands and their decodings

The commands decoding is partial.
The following table gives the commands planned by the controller with their related hexadecimal code.
The bits of each command entering in the decoding network are underlined:

Command	Hexad.Code	b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	Notes
General Reset	45	X	X	X	X	X	1	0	1	These commands do not occupy the controller
Operator Call	43	0	1	0	0	0	0	1	1	
Positioning	4A	0	1	0	0	1	0	1	0	
Check	46	0	1	0	0	0	1	1	0	
Return to home	47	0	1	0	0	0	1	1	1	These commands occupy the controller
Write	42	0	1	0	0	0	0	1	0	
Read	40	0	1	0	0	0	0	0	0	
Check	4E	0	1	0	0	1	1	1	0	
Select. Adv.		X	X	X	1	X	X	X	X	Command used only for the diagnostic
Select. Adv.		1	X	X	X	X	X	X	X	

The CPU sends the commands to the subsystem controller under the form of 8-bit characters.

Every command code is preceded by another 8-bit character specifying the name of the unit to be selected, so every command will consists of at least two characters.

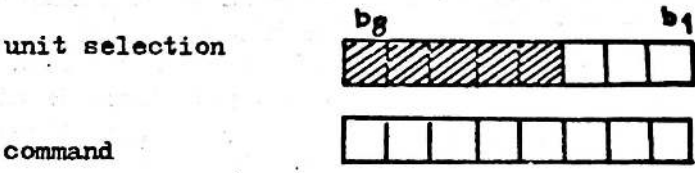
The addressing and positioning commands need, though, additional information, which will be sent from CPU always by means of 8-bit characters.
A wrong or incoherent command sent from CPU to controller because of an error in transmission or for a program error does not stop the controller.
A command will be rejected if one of the following causes occurs:

- controller busy;
- selected unit busy or in manual or in out-of-service or not existing;
- command with wrong check bit.

4.2.3. Commands not occupying the controller

4.2.3.1. General Reset

a. Format



b. Function

This command causes the general reset of the controller. Beside by the diagnostics, it is used by software to remove the out-of-service signal (MARET) when this has been caused by the fact that the service areas written on disk have not been recognized.

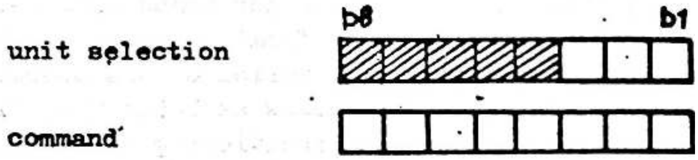
c. Signals to the interface:

CAPET : improbability. The command is always accepted by the controller even if this signal should be present at the end of the command itself.

ERCAT : check error on the command.

4.2.3.2. Operator's call

a. Format



b. Function.

It causes the switching on of the light signal "file alert" on the command panel of the selected unit.
This occurs giving simultaneously to the unit the read and erase gate.

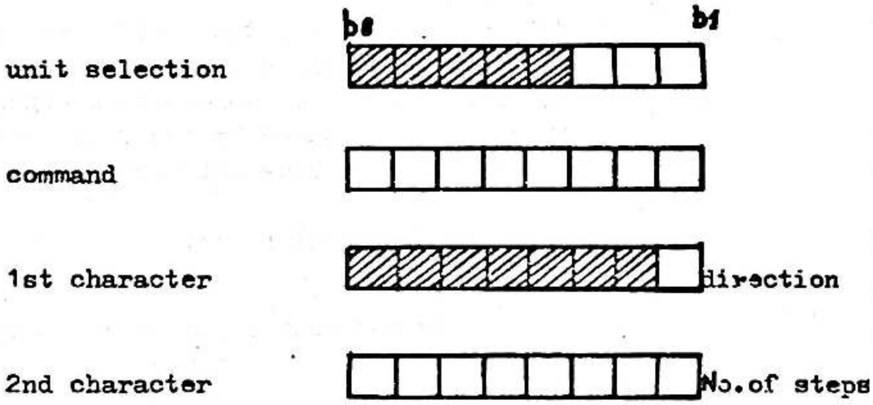
On the interface towards C.P.U. there will be the signal of unit in manual and in out-of-service.

c. Signal to the interface.

MARET : command consequence
SECOT : command consequence
ERCAT : check error on the command
CAPET : if the command has been rejected.

4.2.3.3. Positioning

a. Format



b. Function.

It receives from C.P.U. and sends to the selected disk unit the number of steps that the heads must move and the execution mode.
The positioning is performed in off-line, therefore the unit which is performing such command will show as being busy for all the period of the operation, while the controller will show as being free; it is possible to overlap as many positioning as are the units. If the characters which follow the command code present a wrong check, the positioning does not occur and channel error is signaled.

c. Direction.

Of this character only the less significant bit (b_1) is used to indicate if the unit heads arm must move forward or back.

b_1 = 1 Movement forward (towards the center of the disk)

b_1 = 0 Movement reverse.

d. Step number.

This character indicates the number of steps (in binary code) of which the heads arm will have to move. There is on the controller no check forbidding to send to the unit a number of steps beside the allowed limit positions.

e. Criteria of end.

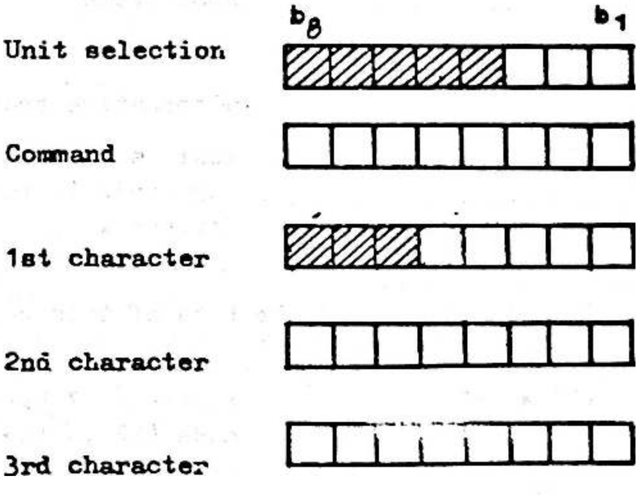
The command end is always decided by the controller and is sent to C.P.U. after having received the 2nd character.

f. Signals to the interface.

CAPET : if the command has been rejected
ERCAT : if an odd parity error has occured on the command or on one of the two characters exchanged.
TESET : incomplete positioning if the heads-holding arm has gone beyond the allowed cylinder set.
INEST : OR of the "Seek complete" signals from DSU.

4.2.3.4. Addressing

a. Format.



b. Function.

This command stores in the controller the execution mode of a subsequent data transfer command and the initial address from which the transfer will occur. The addressing command does not occupy the controller and does not entail any operation by the disk unit.
An odd parity check is performed on the characters received from C.P.U.

c. 1st character. The significance of the bits of this character is the following :

b8 ÷ b6		not used
b5	= 1	characters in the 6 bit format
	= 0	characters in the 8 bit format (when operating on heads b5 must be = 0)
b4	= 1	transfer related to the heads
	= 0	transfer related to data
b3 and b2		indicate the contents of the track indicator related to the track selected by the subsequent characters.

Precisely it is :

b3	b2	
0	0	good track
0	1	faulty track
1	0	alternative track
b1		most significant bit of the binary code indicating the cylinder name.

d. 2nd character.
The significant of the bits of this character is the following:

b8 ÷ b2	remaining 7 bits of the cylinder code (b2 is the bit with less weight)

b1 most significant bit of the binary name of the head on which to operate.

e. 3rd character.

The significance of the bits of this character is the following :

b8 ÷ b5 remaining 4 bits of the binary name of the head (b5 is the bit with less weight)

b4 ÷ b1 name in binary of the sector on which to operate.

f. Criteria of end.

The command end is always decided by the controller and it is sent by C.P.U. after having received the 3rd character.

g. Signals to the interface.

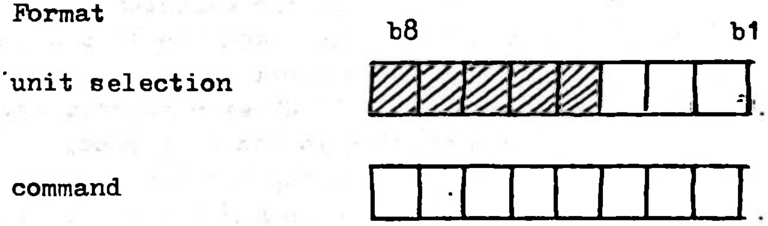
CAPET : if the command has been rejected

ERCAT : if an odd parity error has occured on the command or on one of the three exchanged charac - ters.

4.2.4. Commands occupying the controller

4.2.4.1. Return to Home

a. Format



b. Function

The controller transmits the command to the selected unit; this, first, brings the head-holding arm outside the disk surface, then it makes it move up to track 000.

This command serves to set the head-holding rack in a known position, independently from the previous position and occupies the controller for a period of time which

is below 3 µs, then the operation is continued off-line from the unit.
It resets the signal of "seek incomplete" (TESET)

c. Signals to interface.
CAPET: if the command has been rejected
ERCAT: if an odd parity error has occured on the command.

4.2.4.2. Write

a. Format

	b8							b1
unit selection	▨	▨	▨	▨	▨			
command								

b. Function

It transfers from CPU towards the selected unit the characters following the commands.
The characters are written on disk according to the procedures specified by the previous addressing command.

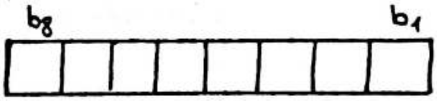
b_1 - write headers.

Starting from the "index mark", on the track corresponding to the selected head, the Home Address, the Record Zero and the 10 track headers (including all the service and check zones) are written in sequence. All "0" with correct cyclic code (all "1") are written in the data zone.
3 characters for the Home Address, 3 characters for the Record Zero and 3 characters for each one of the headers (for a total of 36 characters) are requested from the Central Processor.
The formats of the groups of three characters to be written in the Home Address and Record Zone are the following :

	b8							b1
1st character	0	0	0	0	0	1		

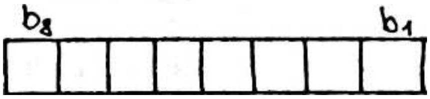
in b_2-b_1 track indicator
b_8-b_3 fixed configuration 00001

2nd character



in b_8-b_1: cilinder address

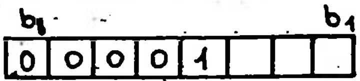
3rd character



in b_8-b_4: head name;
in b_3-b_1: fixed configuration 000

The format of the groups of three characters to be written in the 10 headers the following:

1st character

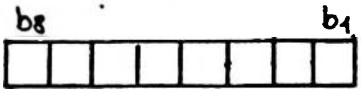


b_8 - b_4 = fixed configuration 00001
b_3 - b_2 = track indicator
b_1 = most significant bit of the binary name of the cylinder

2nd character

b_8 - b_2 = remaining 7 bits of the cylinder name (b_2 is the bit with less weight)
b_1 = most significant bit of the binary name of the head.

3rd character



b_8 - b_5 = remaining 4 bits of the head binary code (b_5 is the bit with less weight)
b_4 - b_1 = binary name of the sector.

All the headers of a track my be written with a command. The end is decided normally by the Central Processor.

If the characters sent exceed the track last sector header, the end is sent from controller after the writing of the last character of such a header.
No check is made on the written header characters.
The operation is accomplished under the control of the Central Processor until the end of the transfer.
If the transferred information do not complete all the headers, the controller continues the writing until the end of the track writing headers and data with all bits "0".
At this point controller and unit are available.

REMARK

Binary weights of the 5 bits indicating the head code of the DSU 157

b_5 (most significant) = 10
b_4 = 8
b_3 = 4
b_2 = 2
b_1 (less significant) = 1

No control is performed on the written header characters structure.
The end is always signaled by controller upon reception of the 36th character.
No transfers with length below 36 characters are allowed.

b_2 - Write data.

The data may be written in 6-bit or 8-bit mode as specified in the immediately previous addressing command.
The interested header is searched for on the track corresponding to the selected head, checking also that the written track indicator corresponds with the one contained in the addressing information supplied by the CPU and checking the cyclic code of the written header.
If this operation has had a positive result and therefore no positioning error has occured, the data arriving from CPU are written.
The passage from a sector to the subsequent occurs automatically for sectors belonging to the same cylinder.
The end of transfer is decided normally by the C.P.U. but if the length of the last transfer exceeds the last character of the last sector of the cylinder, the end is sent by controller together with the signal of end of cylinder (FISET).
The controller provides for the transfer interruption when, passing from a sector to the subsequent and checking the header, it detects a track indicator different from the previous one or a consecutivity error or a cyclic code error on the header and when it does not recognize the initial sector within one revolution and a half of the track under the selected head.
The failure in recognizing one or more service zones written on disk (Address Mark, etc.), necessary to the correct performance of the controller, causes, at the end of the operation, the signal of out-of-Service, which can be reset by a subsequent command of General Reset.

In all the cases in which the end is generated by controller, this exchanges with C.P.U. a character in excess of those effectively written on disk.
If the last sector interested by the instruction has not been completed; the controller provides to write "0" until the sector itself is filled out.
During this time, both the controller and the unit are busy.
In the 8-bit mode data writing, all the data of each character sent from C.P.U. are written unchanged; in the 6-bit mode, the first 6 bits of every character are written unchanged and bits b_7 and b_8 are ignored.

c. Signals to the interface at the end of the command.

CAPET : if the command has been rejected.

ERCAT : if a check error or a synchronization error has occured on the information from CPU (in 6-bit mode no synchronization checks are performed).

PEOOT : if the No. of characters sent from C.P.U. is lower than the sector capacity, PEOOT stays absent until the completion of the sector itself.

EGOLT : address consecutiveness or positioning error

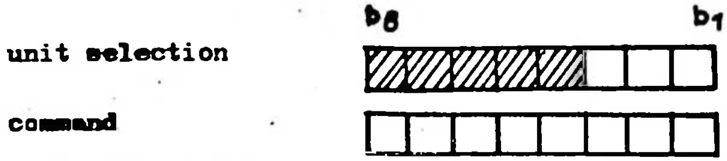
IGOLT : when the track indicator read is different from the one of the addressing.

MARET : no Address Mark has been found or an out-of-service condition has occured on the unit.

FISET : end of cylinder or end of alternative track.

4.2.4.3. Read

a. Format



b. Function

It transfers from the selected unit to CPU the characters read from disk according to the procedures specified by the previous addressing command.

b_1 - Read Headers

Starting from the "index mark" on the track corresponding to the selected head, the Home Address, the Record Zero and the track headers are read in sequence.
Three characters for the Home Address, three characters for the Record Zero and three characters for each header read are sent to C.P.U.
The structure of the three characters is as the one seen for the head writing.
The CPU normally commands the end; if this last one does not occur before the last character of the header of the last sector, the end is determined from controller.
Should in the interval between two subsequent "index marks" all the headers not be read the controller provides to signal EGOLT.

b_2 - Read data

The data may be read in 6-bit or 8-bit modes, as specified by the previous addressing command.
On the track corresponding to the selected head, the addressed header is searched for with the same procedures as seen for the data writing case.
If this operation has had a positive result and therefore no positioning error has occured, the controller reads the data from disk and transfers them to CPU for a length which may be equal to the cylinder capacity.
The end of the transfer is normally decided by the C.P.U., but if the length of the transfer exceeds the last character of the last sector of the cylinder, the end is sent by the controller together with the end of cylinder signal (FISET).
The controller provides to interrupt the transfer when passing from a sector to the following one

and checking its header, it detects a track indicator different from the previous one or a consecutiveness error or a cyclic code error on the header and when it does not recognize the initial sector within a revolution and a half of the track under the selected head.

The failure in recognizing one or more service zones written on disk (Address Mark, etc.) necessary for the correct performance of the controller, causes, at the end of the operation, the signal of out-of-service, which can be reset by a subsequent command of general reset.

In all the cases in which the end is sent from controller, this exchanges with the CPU a spurious character in order to give the signal of end.

If the reading of the last sector interested by the instruction is not completed, controller and unit stay busy until the cyclic code of this sector has been checked.

In the 8-bit mode data reading the read bits are sent unchanged towards C.P.U.; in the 6-bit mode data reading, the controller provides to form again the 8-bit information to be sent to the interface expanding the information in the following way: the first 6 bits (AIFUT-FIFUT) remain unchanged while the 7th bit is equal to the complement of the 6th (GIFUT = $\overline{\text{FIFUT}}$) and the 8th bit is equal to the 6th (GIFUT = FIFUT).

b_3 - Initialization reading

With the signal of system general reset, the abnormal or error conditions are reset; they are set in 8-bit mode, operation on data and the controller addressing registers are forced in order to address the sector "0" of the track "0" of cylinder 000, with "track indicator" set to indicate "good track". After having sent to the controller the general reset, a read command will be sent on the first unit without having it preceded by the addressing command.

At this point the C.P.U. which is ready to perform a data input operation with packing, starts to receive from the controller the even characters written on disk (2nd, 4th ..... 2nth character). The transfer is terminated by the controller after having transferred all the even characters of sector 0 and 1, if it had not been terminated previously by C.P.U.

c. Signals to the interface at the end of the command.

CAPET : if the command has been rejected.

ERCAT : if a check error has occured on the command or a synchronization error on data (in 6-bit mode no synchronization checks are made).

PEOOT : if the number of character to be read is less than the sector capacity, PEOOT is absent until the completion of the sector itself.

EGOLT : positioning or address consecutiveness error.

IGOLT : when the read track indicator is different from the one of the addressing.

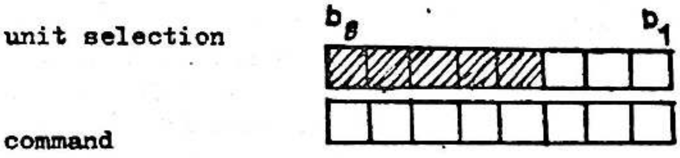
MARET : no Address Mark has been found or an out-of-service condition has occured on the unit.

FISET : end of cylinder or end of alternative track.

SEGET : when an error occurs in the cyclic code of the header or of the data.

4.2.4.4. Verify

a. Format



b. Function

It compares, bit by bit the characters sent from C.P.U. with those read from disk, according to the procedures specified by the previous addressing command. As far as the CPU is concerned, this command behaves as a writing command; as far as the disk unit is con cerned it behaves as a read command.

b_1 - Headers verify

The operation starts always from the Home Address of the track corresponding to the head selected by the previous addressing command.
The C.P.U. normally commands the end; if this last one does not arrive before the last character of the header of the last sector, the end is determined by the controller.
If in the interval between two subsequent "index mark" all the headers are not read, the controller provides to signal EGOLT.

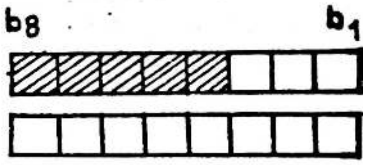
b_2 - Data verify

The initial header is searched for as seen in the operations on the data of the previous instructions; when it has been found and therefore no positioning error has occured, the controller starts the data reading on disk.
The information read are compared, bit by bit, with those arriving from C.P.U.; if the comparison is not verified even for one bit only, or if the cyclic code associated to the data on disk is recognized as being wrong, a comparison error is signaled (SEGET).
The transfer length has the same limits seen for the reading and writing.
The transfer end and the signals are the same as for the writing.

4.2.5. Commands used only by the diagnostics

4.2.5.1. Selector advance

a. Format



b. Function

The command makes the diagnostics counter FE move forward of one position, causing the showing of its decodings.

c. Signals to the interface

Besides those which could be enabled by the decoding of FE present at the end of the command, there could be also the CAPET and ERCAT signals due to the reception of the command itself.

4.3. Program limits description

4.3.1. General reset

The general reset command must be used only to remove the signal of out-of-service (MARET) when this is due to the fact that the service zones written on disk are not recognized; this case of out-of-service is easily detectable as, when it occurs, the signal of manual (SECOT) must not be present.

4.3.2. Positioning

a. The controller does not perform checks on the position reached after a positioning command.

At the beginning of the commands of writing, reading and verify of data in searching for the header addressed previously, the check of correct positioning is also performed.

b. At the end of a positioning command, it is necessary to check the TESET signal, which, if present, indicates that an incomplete positioning has occurred.
The recovery is possible sending to the disk unit a Return to Home command or acting on the command panel of the unit itself.

4.3.3. Addressing

The addressing command must always be sent to the controller immediately before every write, read and verify command; this also if the addressing does not vary with respect to the one sent previously.
In all the operation on the headers, the characters format must be 8-bit mode.

4.3.4. Headers writing

a. The headers of every track must be numbered in consecutive and increasing order as also the tracks of a same cylinder.
Should this procedure not be complied with when operating on blocks with a length which exceeds the capacity of a sector in the passage to the subsequent sector a headers consecutiveness error (EGOLT) is signaled and the operation is interrupted (para.6.2.6.9.1) to the contrary, this does not occur when the blocks have a length which is less than the maximum capacity of the sector on which the operation is done.

b. It is necessary to write also the headers of the cylinder-001 (the cylinder before the 000) with a cylinder code different from the 203 allowed, as, because of a wrong positioning, the head-holding arm of the disk unit may be positioned on such a cylinder without giving to the controller any signal.

If such a case occurs and the headers are not written, the write, read and data check commands will not be performed and the controller behavior will be the same as for a faulty disk-pack.

4.3.5. Headers verify

The number of characters which are sent to the controller in this instruction must always be a multiple of 3 characters, otherwise there is the risk of not performing completely the comparison between the data sent by CPU and those read from disk, or some spurious synchronization errors (ERCAT) may occur.
The verify and header read operations may be done only immediately after the writing of the headers themselves or, if applied after having written the field reserved to data, must be limited to the Track Header.

4.3.6. Initialization

Before an initialization read operation, in order to avoid a positioning error (EGOLT), the head-holding arm will have to be positioned on cylinder 000, thing that occurs after the assembly of a disk pack and the starting of the unit. Only the even characters written on disk are transferred to CPU (2nd, 4th ..... 2 nth character)

4.3.7. Resetting of "Seek Incomplete" signal

Between the showing up of the "Seek Incomplete" signal (TESET para. 4.4.10) and the sending to disc-handler of the command "Return to Home" a minimum time of 15 msec. must elapse.

4.4. Status information

The information sent from controller to CPU are the following:

4.4.1. PEOOT : Availability

The signal indicates that the controller and the selected unit are free and in condition to accept a command.
This signal is absent, independently from the selected unit, during the write, read, check and return to home commands performance.
The signal is absent when the selected unit is performing a positioning.

The absence of this signal may last more than the time strictly necessary to the effective transfer of characters, and in particular:

- during the writing of data or headers, it is absent up to the sector completion;
- during data reading/verify, it is absent up to the completion of the sector.

This signal presence makes all the other states sent to the processor effective.

4.4.2. SEGET : Unit error

The signal is present when in the controller one of the following errors has been detected:

- of cyclic code on the characters read from disk during read and verify (ERCE);
- error in the check of equality between the characters sent from C.P.U. and the characters read from disk during verify phase (ERDA).

This signal is reset by clear, by the general reset command and by the reception of a read, write or verify command accepted by the controller.

4.4.3. EGOLT : Positioning error

The signal is originated during data write, read or verify phases in the following cases:

- the address stored in the controller by the addressing command is not coincident with any of the headings of the selected track which have a correct cyclic code;
- no consecutiveness of two adjacent addresses in operations implying a transfer with a length exceeding the sector capacity;
- the track indicator of one sector is not coincident with the one supplied with the addressing command.

This signal is reset by clear, by the general re set command and by the reception of a read, write or verify command accepted by the controller.

4.4.4. IGOLT : "Track indicator" error.

The signal shows during data write, read and verify when:

- the track indicator of a sector is not coincident with the one supplied with the addressing command and the cyclic code of the header to which it belongs is correct (TIDI).

This signal is reset by clear, by the general reset command and by the reception of a read, write and verify command accepted by the controller.

4.4.5. FISET : End of cylinder

The signal shows during data write, read and verify phase when:

- the length of the transfer is such that the operation goes beyond the last sector of a cylinder;
- the length of the transfer is such that the operation goes beyond the last sector of an alternative track.

This signal is reset by the clear, and by the reception of a read, write or verify command accepted by the controller.

4.4.6. MARET : Out-of-service

The signal is present together with the SECOT signal:

- if an operator call command has been sent to the selected unit;
- if the selected unit is in out-of-service or not existing.

The signal is present while the SECOT signal is absent:

- if the controller power supply is powered-off because of a malfunction;
- if during a data write or read or check operation, the initial transfer on a track must continue on the subsequent and on this last one the service area indicating the header beginning (Address Mark) is not recognized. What above mentioned, may be due to the fact that the selected track is faulty just in the areas reserved to the service information or to a general read error (which may be recoverable or not);
- if during headers reading or verify the end of track is reached without having read all the 10 written heads.

If the cause of this signal is one of these two last ones it can be removed by means of the immediate command of General Reset, otherwise eliminating manually the reasons which have caused them.
This signal is removed during the selection for a periods of 5.7 µs.

4.4.7. SECOT : Unit in manual

This signal is generated by some conditions which generate the MARET signal (refer to 4.4.6.).

4.4.8. CAPET : Improbability

The signal is present when the command has been rejected.
The command is rejected when:

- it is sent with controller or unit busy;
- it is sent with wrong check;
- it is sent to a unit in out-of-service or in manual;

- it is sent to a non-existing unit.

All the cases above listed make the signal show immediately after the reception of a command, which will not be performed.
The signal is reset with the next command sent to the controller.

4.4.9. ERCAT : Channel error

This signal shows for one of the following reasons:

- disparity error on the information (data and commands) received by C.P.U.;
- synchronization error during the information exchange with the CPU (the synchronization check is performed by the controller only in the 8-bit mode).

It must be noted that when such an error occurs on the command characters it causes in any case the non-performance of the command itself.
This signal is reset by the next command sent to the controller.

4.4.10. TESET : Seek incomplete

This signal is determined by the sending of the signal "seek incomplete" by the selected disk unit and shows when, after a positioning command, the head-holding arm is positioned outside the allowed set of cylinders (000 - 202).
To remove such a signal either act manually on the command panel of the disk unit or send by the C.P.U. a command of Return to Home.
Between the showing up of TESET and the sending to disc-handler of the command "Return Home" a minimum time of 15 msec. must elapse.
This signal provides always to remove the signal of busy arriving from the disk unit and then to free the controller.

4.4.11. **INEST :** Interruption

It shows at the end of every positioning of the head holding arm of the disc unit.
The OR of the signals arriving from the various units is sent to the Central Processor.
The signal is reset with the next read verify headers or write read verify data or positioning command.

5. OPERATION AND MAINTENANCE CHARACTERISTICS

5.1. Operating panel

The DSC 157 does not have an operating panel.

5.2. Maintenance panel

The DSC 157 does not have a maintenance panel.

5.3. Failures diagnosis

For the failure diagnosis during a first phase special diagnostic programs are used and during a second phase, for the systems with a test device (VAR 580), the diagnostic device VAR 583 described in drawing No. 14623102 is used.
The diagnostic programs used are described in drawings No.

5.4. Alert conditions

The controller ventilation group is provided with a protecttion device for no ventilation whose intervention causes the total switching off of the system.

6. OPERATIONS THEORY

6.1. Description at general block diagrams level

Referring to the general block diagram, dwg.No. 78B103722 the controller logic may be divided as follows:

6.1.1. BU register

It is a register consisting of 9 FF (BU00 - BU08) which serves as a buffer during exchanges with C.P.U.
The information which are stored in this register are all the commands and the data transmitted by CPU towards controller and the data transmitted by controller towards CPU during the read phase.

6.1.2. Check network

It is a logic network connected with the BU register which serves:

- in input from CPU to check the odd parity of the information received on the distribution channel;
- in output towards CPU to construct the odd parity bit of the information transmitted on the collector channel.

6.1.3. NA Register

It is a register consisting of 3 FF (NA00, NA01, NA02) which serves to store the code, arriving from CPU, related to the disk unit which will have to be selected.

6.1.4. NU Register

It is a register consisting of 3 FF (NU00, NU01, NU02) which serves to store the code, arriving from the NA register, related to the unit on which the operation is presently occuring.

6.1.5. MA Register

It is a 8 FF register (MA00 - MA07) shift connected:

- in writing it allows the passage from the parallel information arriving from the BU register to the serial information necessary to write on disk;
- in reading it serves to apply the inverse case, i.e. the passage from the serial information arriving from disk to the parallel one to be transmitted to C.P.U.;
- in checking, it allows the passage from the parallel information arriving from the BU register to the serial information necessary to perform the comparison with the information arriving from disk;
- in the operation on data, during the header search phase, it serves to serialize the contents of registers TI,CI,HE and SE in order to perform the comparison,bit by bit, with the information arriving from disk.

6.1.6. SH Register

It is a 12 FF register (SH00 - SH11) shift connected:

- in writing it serves to build up the cyclic code to be written at the end of every header and of the data;
- in reading or checking, it serves to check that the cyclic code arriving from disk and related to data or to the headers is correct;
- in case of search of the header during operations on data it serves to check the cyclic code of the header under exam.

6.1.7. TI Register

It is a 2 F.F. register (OOTI, O1TI) which serves to store the track indicator sent with every addressing command; it is used in the operations on data during the header search phase of every sector.

6.1.8. CI Register

It is a 8 F.F. register (CI00 - CI07) which serves to store the name of the cylinder on which the operation is going on.
This register is loaded during an addressing operation and it is used in operations on data during the phase of header search of every sector.

6.1.9. HE Register

It is a 5 F.F. register (HE00 - HE04) which serves to store the name of the selected head on the disk unit; it is connected to a counter and it is cyclic from 0 to 19 in the passage from one track to the subsequent, the above mentioned counter counts +1.
It is loaded during an addressing operation and used, when operating on data, during the phase of header search of every sector.
For the binary weigts of the bits indicating the head code see par. 4.2.4.2. b_1.

6.1.10. SE Register

It is a 4 F.F. register (SE00 - SE03) which serves to store the name of the sector on which the operation is going on, it is connected to a counter and it is cyclic from 0 to 9.
In the passage from a sector to the subsequent, the above mentioned counter counts +1.
It is loaded during an addressing operation and used, when operating on data, in the sector search phase and, when operating on the headers to count the sectors within every track.

6.1.11. Discriminations and phase logic -PLO

The discriminator is a device which has the purpose to create the gates necessary to divide the informations bits from the clock bits of the continuous sequence of bits which show on the controller input channel.
If the two output lines of the discriminator are inverted the logic for phase changing provides to correct them (ref. timing No. 78B103727 page 14).
This logic analyzes constantly the output line of the clock bits and intervenes when these last ones do not show for a time equal to about 2 characters.
Its intervention consists of losing a count to the DIVI F.F. which generates the discriminator gates, so all the subsequent gates will be moved over of 400 ns with respect to when the phase was wrong.
The PLO is a variable frequency oscillator which oscillates according to the average frequency of the pulses related to the information read from the disk; it is in condition to feel only the slow variations (ref. timing No.78B103727 page 13).
For detailed information on this device, refer to PHOS D board description n° 30004124.

6.1.12. Command and mode FF

- The command FF are nothing else but a series of FF which store the code of the commands which arrive from CPU for all the time necessary to perform the command itself. All these FF are not set if the command is rejected.
- The mode FF have the purpose to store some information arriving from CPU which will then be used by the controller to better define the performance procedures of some commands.

6.1.13. Comparison and headers recognition logic

This logic always intervenes when operating on data and when searching the header of the initial sector, or the one of the subsequent sectors if information are exchanged exceeding the maximum sector length.

Beside detecting the service area characterizing the beginning of every header (address mark), it performs the bit by bit comparison between the information arriving from disk related to the header under exam and the one stored in the controller register with the addressing command.
In the verify operations it performs also the comparison between the information arriving from disk and those arriving from CPU stored from time to time in the MA register.

6.1.14. Write oscillator and synchronization logic

It is a quartz oscillator whose main purpose is to supply all the timings necessary to the controller in the write phase.
It oscillates freely as soon as the power supply voltages are supplied, then a synchronization logic on the controller provides to condition the outputs of the oscillator itself and to synchronize them every time they are to be used.
In addition, it clocks the bit counter (BI) and the character counter (DA) which are also used to measure the wait periods which are needed in some instruction.

For more detailed information on the quartz oscillator (TERE) refer to specifications No. 30074089.

6.1.15. Control logic

Under this name there is all the logic which serves to check the performance of all the operations driven by C.P.U. and to connect one another the various elementary logic parts.

6.1.16. Bit counter (BI)

It is a counter consisting of 3 FF (BI00, BI01, BI02) which counts cyclicly from 0 to 7 or from 0 to 5 depending on the count mode determined by the mode register.

In the addressing and positioning, it counts the characters that the CPU sends to the controller while in the read, write or check operations, its counts are associated to the bits of every character.
In read and check, the counts are done by an internal trigger derived by the serial information arriving from disk handler, while in writing they are done by the quartz oscillator described sub point 6.1.14.
A forcing on every FF is planned in order to make the counter assume, in testing phase, any configuration among the possible ones.

6.1.17. Character counter (DA)

It is a binary counter with 9 FF (DA00 - DA08) whose countings occur at every recycle of the BI counter.
Its purpose is to follow the read, write and check instructions in their performance within the track; its decodings go to condition the main FF of the check logic.
A forcing is planned on all the F.F. except on DA02 so that the counter in test phase may assume the main configurations among the possible ones.

6.1.18. Logic for the diagnostics

It consists of a 4 FF counter (FE00 - FE03) whose decodings are used in the following way:

- to enable the sending on the collector channel of the C.P.U. of some main FF of the controller;
- to force to "1" or to "0" some signals internal to the controller and thus to avoid the manual operations of forcing by means of movable strappings;
- to enable some special logics;
- to send some signals internal to the controller on unused signals of the interface towards C.P.U.

The counts of this counter are performed upon command from C.P.U. as described in para. 6.3.7.2.

6.2. Description of functions and performances at intermediate block diagram level (ref. drawing No.78B103723)

The controller performs the following main functions:

- accept by CPU and send to the disk handler the head positioning commands;
- accept by CPU and send to the disk handler the addressing commands;
- perform the write commands;
- perform the read commands;
- perform the check commands;
- perform the operator's call commands;
- check the various operations performance;
- select and transmit to CPU the states of the connected units and of the controller itself;
- perform some special diagnostic functions.

The controller performs the following checks:

- odd parity check on all information from C.P.U.;
- check that the selected sector is on the positioned track;
- check that the sectors addresses are increasing and consecutive;
- check the cyclic code of the data read on disk;
- check that the data transfer length does not exceed the maximum allowed length.

During the read and check commands performance, the controller timing is driven by the disk handler; during the write command performance, the timing is driven by the controller itself.

6.2.1. General reset

All the controller storage circuits which at the beginning of the operations must be in a given status, are set by the following signals:

- CAGUT : clear from CPU;
- MARET : signal of out-of-service to CPU;
- VIDIN : pulse generated by the trigger accompanying the command;
- CADIN : pulse generated by the general reset command sent by CPU;
- RESEN : pulse generated at the end of the instructions which occupy the controller.

These signals are suitably grouped in OR depending on the FF to be set.

6.2.2. Disk handler selection (ref. timing 78B103727 page 1)

At the beginning of every dialogue the C.P.U. selects the unit on which it wants to operate sending to the controller the signals AEBET, PUOOT and on the distributor channel the binary code related to the unit name.
The controller performs no check on this last information.
The register NA and the register NU with the respective decoding network are interested in the selection operation.
Three possible cases are distinguished essentially:

- selection with controller free;
- selection with controller busy;
- double selection.

6.2.2.1. Selection with controller free

The information arriving from the distributor channel is stored in the 3 FF of the register NA by the signal PUBE and if the controller is free after an interval established by the one-shot circuit EBEA, the content of the register NA is transferred in the register NU by the pulse NANU.
At this point, the code of the name of the unit on which to operate contained in the register NU, is sent to the interface towards the disk handler, the unit with a plug corresponding to the code sent to interface will be selected.

The controller provides to declare itself busy from the moment in which it receives the selection for a period of time established by the one-shot circuit RISO and to remove for that time the out-of-service signal (MARET) from the interface towards C.P.U.

6.2.2.2. Selection with controller busy

The information arriving from the distributor channel is stored in the 3 FF of the register NA by the signal PUBE and, if the controller is busy, only after its freeing the content of the NA register is transferred in the NU register through the pulse NANU generated by the trailing edge of ORTA.

The controller in this case declares itself still busy for a period of time defined by the one-shot circuit RISA.

6.2.2.3. Double selection

This case occurs when the controller is performing a selection, and is therefore busy, and the CPU sends another one when the one-shot circuit RISA is still at 1.
At this point, there will be two loading of the register NU which at the end will contain the code sent with the last selection.
The controller stays still busy for a period of time defined by the OR of the one-shot circuit RISA and by the one-shot circuit RISO; this last one has begun to work at the reception of the 2nd selection.

6.2.3. Command acceptance (ref. timing 78B1C3727 page 2)

The transmission of a general command from C.P.U. to controller occurs sending on the distributor channel the code associated to it, accompanying it with the pulse TU20 and with the conditions of VICU and FINUN.
The controller, after having stored with the pulse FUDI the command code in the register BU, proceeds to some checks before setting the corresponding FF which stores it.

The main checks which are performed when receiving every command are:

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- check the command code: when the signal CEGE coming out from the check network is at level logic "0" it means that the check is correct;
- check that the selected unit is not in manual: if the signal SECO is at logic "1" level, it is in manual status.

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- check that the controller and selected unit are not busy: if the signal PEOI is at logic level "1", both are in the free status.

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The result of the last two checks is stored for the whole length of the reception of the command in the F.F. MOCU, so the set status of this FF or the possible check error determine the raising of the FF command error (ERCO), the inhibition of the pulse to set the command FF (TUCO) and the CAPET signal to the interface.
The check error causes also the raising of the channel error signal (ERCAT).
If none of the controls give positive results the pulse TUCO is generated which stores the command code in the related FF for the whole length of the instruction itself.
The trigger accompanying the command (TU20), if the controller and the selected unit are free, generates a pulse (VIDI) which goes to reset the FF, which at the reception of the command must be at logic "0".
The commands of general reset and the one of selector advancing (diagnostics) are never rejected by the controller even if at their end the signal CAPET might be present.
At the end of the acceptance phase, the controller provides to send to CPU the pulse of reception (TE30T).

6.2.4. Commands storage

The various commands planned by the controller logic pass through a decoding network, depending from the BU input register and afterwards, if accepted, they are stored in the respective command FF.
The table below gives the planned commands with the name of the decoding associated to it and the one of the flip-flop which stores them:

Command	Decoding	Flip-flop
- operator's call	DECO	COPE
- positioning	DEPO	POSI
- addressing	DEIN	INDI
- return to home	DERO	RETO
- write	DERE	REGE
- read	DELE	LEGE
- check	DEVE	VERE
- general reset	CADI	
- selector advance	TUDI	

The general reset and selector advance commands are not stored by the controller; their decodings in AND with pulses derived by TU20 are used.

The FF for inizialization reading (LEIN) is set at 1 with the reset command and reset at every accepted addressing command.

6.2.5. Performance of the commands which do not occupy the controller

6.2.5.1. General reset command (XXXXX101)

When this command is received, the controller generates a pulse (CADI) which is the AND between the command code

decoded directly by the information arriving from the distributor channel and the DIEU pulse derived by the accompanying TU20.
This command does not imply any character exchange with CPU and serves to reset some FF of the controller, in particular it resets the DIRO FF (MARET) when with this signal there is not SECO.
The controller never rejects this command even if at the end of the command itself it should signal CAPET to the CPU interface.

6.2.5.2. Operator's call command (01000011)
(ref. timing 78B103727 page 2)

The code of this command is stored in the COPE F.F.
The following signals are then sent to the selected disk handler:

- on the line BUS1U the read gate
- on the line BUS4U the erase gate
- on the line SERIU the control pulse generated by the RERU one-shot circuit.

When the disk handler receives simultaneously these signals, it sends to the controller the error signal UNSAU and provides to turn on the light signal "file alert" set on its command panel.
The controller, at this point shows the signals of out-of-service (MARE) and of manual (SECO).
To remove this signal, it is necessary to intervene manually on the disk handler.
This command does not entail any characters exchange with C.P.U.

6.2.5.3. Positioning command (01001010)
(ref. timing 78B103727 page 3)

When this command arrives, the controller provides to store it in the POSI F.F. and to reset the cylinder register set on the disk handler, sending to the disk handler itself the signal SECIU on the tag line concerning the "set cylinder" and no signal on the bus line.

The command received signal is sent to C.P.U. and the first character is requested; it is the one which will have to supply the data concerning the direction according to which the head-holding arm will have to move.
At the arrival of this character which, as all the subsequent is stored in the BU register, the counter BI, which initially has been zeroed, counts +1 and generates the decoding 01BI.
The less significant bit of BU is sent on the line BUSOU of the disk handler accompanied by the signal SFTIU (set head and direction).
The command received signal is given and the second character is requested, i.e. the one concerning the number of steps that the head-holding arm will have to move.
When this last character arrives, the BI counter counts +1 and generates the 02BI decoding.
The controller then sends to CPU the signal of end from outside (FINET) and on the unit bus lines the complement of the BU register accompained by the signal SEDIU (set difference) and it gives the received signal.
The C.P.U. will send the signal of end of instruction (FINUT) so that, if no check or synchronism errors have occured on the characters exchanged, the unit receives the permission to perform the command (SERIU).
This command entails the exchange of 2 characters between the CPU and the controller.
The checks performed by the controller during this phase are synchronism and odd parity checks on the characters received.
If at the end of the command, the head-holding arm is set outside the allowed set of cylinders, the unit sends to the controller the signal "seek incomplete" (SEINU)which provides to signal TESET to the interface with the C.P.U. and to free the controller.

The information that the controller exchanges with the disk handler at every character that the C.P.U. sends it, are given in the Table below:

B1 decoding	TAG Line	BUS Line
00BI	SECIU	
01BI	SETIU	BUSOU
02BI	SEDIU	BUSOU+BUS7U
03BI	SERIU	BUS2U

At the and of every positioning command a [illegible] signal is sent to CPU.

6.2.5.4. Addressing command (01000110)
(ref. riming 78B103727 page 4)

When this command arrives, the controller provides to store it in the INDI FF, to send to C.P.U. the TE30 of command received and the request of the first character which gives to the controller the information related to the mode and the track indicator.
The reception of this character, which as for the two subsequent ones is stored in the register BU, causes the count +1 of the BI counter, which, in this instruction, counts the characters exchanged between controller and C.P.U.
The various bits of BU concerning the first character are transferred in the following way :

- The 1st bit concerning the most significant bit of the binary code indicating the cylinder name in the CI07 F.F.
- the 2nd and the 3rd bit concerning the track indicator in the TI register (00TI, 01TI);
- the 4th bit which, depending whether it is at logic "1" or "0", indicates that the subsequent operation will be respectively either on the headers or on the data in the TETA F.F.;
- the 5th bit which indicates, depending whether it is at logic "1" or "0" that the characters format in the subsequent operation will be with either 6 or 8 bits, in the MOSE F.F.

In addition, the register containing the head name is reset, sending to the unit the bus line BUS3U accompanied by the tag control line and then the received signal and the request for the subsequent character is sent to C.P.U.
The most significant seven bits of this last one (BU01+BU07) are transferred in the correspondent F.F. of the cylinder register (CI00+CI06) and the less significant bit (BU00), concerning the most significant bit of the binary code indicating the head name in the 04TE F.F.
The controller provides right away to send the received signal and to request the subsequent character.
The most significant four bits of this last one (BU04+BU07) are transferred, with the contents of 04TE, in the correspondent F.F. of the head register (HE00+HE04) and the less significant four bits, concerning the binary code indicating the sector name in the corresponding FF of sector register (SE00+SE03). The head code contents in the HE register is

also sent to the disk handler on the lines BUS3U-BUS4U-BUS5U BUS6U-BUS7U accompanied by the tag line SETIU(set head and direction). At this point the end from outside (FINET) is signaled to CPU and the signal FINUT is expected which will end the instruction. This command implies the exchange of 3 characters between CPU and controller. The checks performed by the controller in this phase are synchronism and odd parity checks on the characters received.
The information that the controller exchanges with the disk handler at every character that the C.P.U. sends it are given in the table below:

BI decoding	TAG Line	BUS Line
00BI		
01BI	SERIU	BUS3U
02BI		
03BI	SETIU	BUS3U,BU4U,BUS5U BUS6U BUS7U
04BI		

6.2.6. Performance of the commands occupying the controller

6.2.6.1. Return to home command (01000111)

(ref. timing No.78B103727 page 2)

When the controller receives this command it stores it in the FF RETO and provides to declare itself busy setting the FF GOVO.
Then the line BUS6U accompanied by the tag control line (SERIU) is started towards the disk handler and it lasts for a period of time defined by the one-shot circuit RERU.
The controller provides to free itself by means of the trailing edge of RERU while the instruction goes on off-line.
Only when this last phase will be over a signal will be sent to the interface towards C.P.U. informing that the subsystem is free and therefore it is in condition to accept the subsequent command.
This instruction is immediate and does not imply any character exchange with C.P.U.; in addition it serves to reset the signal of TESET which stores the signal "Seek in

complete", transmitted by the disk handler.

6.2.6.2. Write headers (01000010)

6.2.6.2.1. General

The controller performs this special type of instruction when, at the reception of a write command, the FF TETA is at logic "1".
With this instruction, the previously selected head writes on disk the track format according to the structure defined in para. 4.1.2.
The controller therefore provides to send to the disk handler both the serialized information derived from those transmitted by C.P.U. and concerning the home address, the record zero and the 10 headers and the service areas necessary to the performance of the subsequent operations.
All the timings which serve during writing are derived from a quartz oscillator which oscillates at the frequency of 2.5 MHz (para. 6.1.15.).
Every cell of the pulses sequence written on disk consists always of a bit followed after 400 ns by its clock.
The characters to be written are stored in the register BU and from here are transferred in the register MA when the subsequent character has already been requested, as the C.P.U. will answer always with a certain delay with respect to the request.
The minimum time between TE1OT and TU2OT acceptable by the controller is of 1684 ns.
In this instruction, the FF MOSE indicating the characters format, during the previous addressing instruction must not have been set at logic "1".
The counts of the BI counter and subsequently those of DA are checked by the FF MOTO and MOSE which set the BI counter to count either in 8 or 6 bit mode: in particular during the writing of the service areas the BI counter counts in 6 bit mode.
This instruction implies the exchange of 36 characters with the C.P.U. which are written in groups of 3 according to the structure given in para. 2.4.4.2.b1.
The meanings of the various check FF which intervene are:

USBI : at logic 1 it enables the quartz oscillator outputs and therefore the counts of BI and DA.

GAPE : at logic 1 it enables the writing on disk of zero characters.

COCE : at logic 1 it enables the building up of the cyclic code and the shift of the SH register.

CHEC : at logic 1 the writing on disk of the cyclic code.

RICA : at logic 1 it enables the request in cycle of the characters to be recorded.

MISI : at logic 1 it enables the writing of "1" without clock in the address mark area.

BLOC : at logic 1 it enables one BI counter comit.

SMAB : at logic 1 it enables one MA register shift.

6.2.6.2.2. Initial phase (ref. timing No.78B103727 page 5)

When the write command is received, it is stored in the F.F. REGE; then the FF SETE and USBI are set which serve, the first one, to start the head selection phase through the sending to disk handler of the bus line BUS5U accompanied by the tag control SERIU and the secondone to enable the counts of BI and DA.
At this point, having let elapse a period of time of about 60 μs necessary to the head selection, the FF DEME is set and the "index mark" signal is waited (INDAU) and then the write on disk phase is started.
The time above mentioned is defined by the arrival of decoding 13 of DA (D013).

6.2.6.2.3. Track Header (ref. timing No.78B103727 pages 8, 10)

When the index mark arrives the BI and DA counters are reset and if the initial phase has already elapsed, i.e. the FF DEME is at logic 1 from the previous phase, the FF EDER is set, which characterizes all the writing phase of the Track Header.
Now the FF GAPE is set and the "index gap" writing equal to 43 characters zero starts.
With the decoding D005 of DA DEME is reset and with D041 the first character of the home address is requested to C.P.U. and with the decoding D042 the FF GAPE is reset and the FF RICA is set.

Starting from the decoding D042 6 bits "1" are written on disk; after that the FF MOTO is set, which remains at logic "1" from the decoding D043 to the decoding D046 and characterizes,beside the counting mode of BI, also the writing on disk of the characters concerning the home address.
The character arriving from CPU is stored in the input register BU and subsequently transferred in MA with the pulse BUMA which generally follows the subsequent character request.
From the MA register the character comes out serially in shift mode starting from its most significant bit and it is sent to the disk handler with the frequency established by the quartz oscillator.
The home address writing goes on in the same way for other two characters; the last request relates to the first character of the Record Zero.
The 12 bits related to the Cyclic Code detected by the FF CHEC which stays at logic 1 from the decoding D046 to the decoding D048 are written in sequence after the Home Address.
This information has been calculated making the Exclusive OR between the contents of the most significant FF of MA and the most significant FF of SH for the whole period in which COCE and MOTO are simultaneously at 1 writing the result in the FF ORES and from here in the first FF of the SH register.
The writing of the Cyclic Code is done by shifting the information contained in SH and writing the complement of its last FF (SH11); at the end of the operation the register stays at zero.
The FF GAPE raises again staying at logic 1 from the decoding D048 to the decoding D070, allowing the writing on disk of the 22 characters zero concerning the "data gap" and, right after the 6 bits 1 and the 3 characters concerning the Record Zero followed by their Cyclic Code.
The various FF which have intervened previously, intervene again but set and reset by different decodings.
The last character requested in this phase concerns the first character of the heading of the 1st sector.
Finally 43 characters 1 are written providing, at the end of this operation, to reset the BI and DA counters,to make the sector counter SE (RECO) advance, to reset EDER and to set TRAC.

6.2.6.2.4. Sector (ref. timing No. 78B103727 pages 9 - 11)

This phase is subsequent to the previous one and therefore the information on disk does not undergo any interruption.
In fact, after the "1's"written previously 6 characters zero are written through the FF CAPE which stays at 1 from the decoding D000 to the decoding D005;then the service area called "address mark"is written,consisting of 6 bits "1" with clock,4 bits "1"without clock,2 bits"1"with clock, 4 bits" "1" without clock,and 2 bits "1" with clock.
The writing of this special configuration which will be useful in the subsequent instructions to recognize the beginning of the various headers, is controlled by the FF MISI which inhibits the clock writing.
At this point using the BLOC F.F.,that enable a BI counter count,and the SMAB F.F.,that enable a MA register shift, the first "0" bit of Data Mark is written;then the three characters of the header are written. The first one has been requested during the writing of the Record Zero. In this phase there is also the anticipated request of the first character of the subsequent header.
The interving control FF are the same ones of the previous phase, driven,though, by different decodings.
After having written the cyclic code at the D013 decoding the FF CAPE raises, remaining at logic 1 up to the D035 decoding, allowing the writing of the "data gap". Six bits "1", five bits "0" and one bit "1" forming the "data mark" are written in sequence.
Then, 288 characters "0" followed by the related cyclic code, which in this case consists of 12 bits "1", are written in the field reserved to data.
At this point, the zone related to the sector is completed with 47 characters "1", then BI and DA are set to zero, the sector counter moves forward and the writing starts on the following sector.

6.2.6.2.5. Last sector (ref. timing 78BI03727 page 9)

The writing of the last sector occurs as for the previous ones,only that at the arrival of the last character to be written (36th character) the controller sends to C.P.U. the signal of end from outside(FINET)and blocks automatically the request of the subsequent character.

After having written the whole sector, the controller completes with characters "1" the disk area called "long gap" which is located between the end of the last sector and the arrival of the index mark.
At this point the pulse RESE is generated which ends the instruction freeing the controller.

6.2.6.2.6. Cases of end

The end is always issued by the controller and it is sent to the C.P.U. after the arrival of the 36th character.
If the information transferred do not complete all the headings, the controller goes on to write up to the end of the track writing in the zones reserved to the following headers all zeroes.
These last ones cannot be read in the subsequent phases.

6.2.6.2.7. Signals to the interface at the end of the command

CAPET : when the command has been rejected.

EHCAT : if a check error or a synchronism error has occured on the characters exchanged.

PEOOT : it is absent from the moment in which the command arrives until the completion of the "long gap".

6.2.6.3. Read headers (01000000)

6.2.6.3.1. General

The controller performs this special type of instruction when, upon reception of a read command, the FF TETA is at logic 1.
With this instruction, the previously selected head reads from disk the information written in the areas reserved to the headers.
The controller provides to send to C.P.U. in a parallel mode the finromation derived from those serially read from disk and concerning the home address, the record zero and the 10 headers.

The header read operation may be done only immediately after the writing of the headers themselves or,if applied after having written the field reserved to data, must be limited to the Track Header.
All the timings which intervene in the reading are derived from a delay line which performs its cycle in synchronism with the information arriving from disk.
As these information are subject to frequency shifts due to the disk speed variations both during the previous writing and during the reading under way, at the controller output there is an oscillator (PLO) which modifies its frequency in function of the above mentioned variations and generates the pulses which will serve to the discriminator to form the gates suitable to divide bits one from the clock bits.
As it has already been seen previously in para. 6.1.11., if the discriminator outputs are not correct, the phase changing logic intervenes making the ones (BILE) and the clocks (COLE) go out on the correct lines.
The bits related to the characters to be read are written in the first FF of the register MA and are shifted at every subsequent bit; when a whole character is in the register, its contents, by means of the MABU pulse, are transferred to the output register BU.
At this point, the check bit is generated and the character is introduced together with the accompanying TE20 on the collector channel of the C.P.U.
The counts of the BI counter and, consequently, those of DA are checked by the FF MOTO which depending whether it is at 1 or 0 makes the counter BI count in 8 or 6 bit mode.
The FF MOSE, indicating the characters format, must not have been put at logic "1" by the previous addressing.
The logic meaning of the main FF which control the performance of this instruction are.

USBI : at logic "1" it enables the outputs of the quartz oscillator and therefore the counts of BI and DA.

USBE : at logic "1" it enables the output of the various pulses of the delay line and then the counts of BI and DA.

RIGA : at logic "1" it gives the read gate to the disk unit.

GALE : at logic "1" it enables the discriminator output.

DUZE : at logic "1" it indicates that two characters zero have been recognized at the discriminator output and that, therefore, the output channels of this last one are correct.

ADMA : at logic "1" it indicates that an address mark has been recognized.

MOTO : at logic "1", beside establishing the BI count mode, it enables the shift of the MA register and at the end of every character read the start of the accompanying TE20.

COCE : at logic "1" it enables the construction of the cyclic code and the shift of the SH register.

6.2.6.3.2. Initial phase (ref. timing78BI03727 page 5)

Upon reception of the read command, it is stored in the FF LEGE; the FF SETE and DEME are set which serve, the first one, to start the head selection phase, by sending to the disk unit the bus line BUS5U accompanied by the tag control SERIU, and the second one the waiting phase of track beginning.
Upon the index mark arrival, the counters BI and DA are reset, then the FF EDER detecting the zone concerning the Track Header and the FF USBI which starts the counts of the above mentioned counters, are set.
With the decoding 5 of DA (D005) DEME is reset and with D013, i.e. after about 60 us from the index mark RIGA is set which provides to transmit to the unit the read gate.
At this point the sequence of pulses arriving from the controller provides to start the variable frequency oscillator (PLO), the discriminator and, if the outputs of this last one are inverted, the phase changing logic (refer to para. 6.1.11.).
The discriminator outputs are used only when the PLO is in step and for this purpose, from the moment when the read gate raises to when these outputs are used, a period of time equal to 7 characters must elapse.
The decoding D020 forces in the counters BI and DA the configuration of the first "1" written on disk, the FF GALE is set enabling the discriminator outputs and the

recognition phase of two characters zero on the data line of the discriminator itself starts.

6.2.6.3.3. Track Header (ref. timing 78BI03727page 12)

After having recognized two zero characters (FF DUZE = 1), at the arrival of the first bit 1 on the data line, FF USBE is set, which, for all the period in which it stays at one, allows the delay line to cycle and therefore allows the output of all the timing necessary to read.
During the period elapsing between decoding D043 to decoding D046, the FF MOTO stays at 1, allowing at proper times the loading in the MA register of the three characters of the home address.
This register, which shifts its contents at every cycle of the delay line, serves to re-build the parallel information related to every character.
The MABU pulse is generated at the end of every character and serves to transfer the contents of MA in BU and to start the related accompanying timing (TE20).
The cyclic code is formed on the information read, making the Exclusive OR between every bit and the last FF of SH for all the period in which the FF COCE stays at 1 and writing the result in the FF ORES and from here in the first FF of SH.
The contents of this register at the end of the 3 characters of the home address, if no errors have occured, are equal to the complement of the cyclic code, so continuing the operation of Exclusive OR at the end all FF of SH will be at one.
If this condition is not verified, the FF ERCE is set and SEGET is signaled to the interface towards C.P.U.
The FF MOTO raises with the decoding D071 which stays at 1 up to the decoding D074.
During this time, the characters related to Record Zero are read in the same mode of the 3 previous characters.
At the end of the cyclic code, the SE register moves forward of one position, the FF USBE is reset and the phase of search for the "address mark" related to the header of the 1st sector starts.

6.2.6.3.4. "Address Mark" recognition (ref timing 78B103727page 16).

The "address mark" is a special configuration of bit one and clock bit which precedes all the headers written on disk.
It is written during the header writing phase and consists of: 6 bits one with clock, 4 bits one without clock, 2 bits one with clock, 4 bits one without clock and 2 bits one with clock.
The recognition phase goes on in the following way: when two zero characters have been detected at the discriminator output the clock line output (CODI) is constantly checked by means of a RIRA circuit (refer to specifications 015740150).
The signal ADREN, which is the output of this circuit, stays at zero when at the input there are the clocks and it raises when these last ones are not present for a period of time exceeding its internal period.
If ADREN raises, it means that the first area in which the clocks are lacking has been found, so through the RESU one-shot circuit the pulse MASU is created which STARTS MARC, ONE-SHOT.

If ADREN goes down and raises once more and MARC finds at one, it means that two subsequent clock absences have been detected and therefore the address mark has been recognized and the FF ADMA is set, through the ADRI pulse.

6.2.6.3.5. Headers from the 1st to the 9th sector (ref. timing 78B103727 page 18).

Once the address mark has been recognized (FF ADMA = logic 1), the one-shot circuit FC08 starts, which after having zeroed the counters BI and DA, at the end of its period forces to logic 1 the FF MOTO and PELE and in the above mentioned counters, the configuration related to the first "1" of the subsequent "data mark".
Upon the arrival of the first "1" above, the FF USBE is set and the first FF of MA is set to"1"simulating the first bit of the data mark which otherwise would go lost.

The MA register then receives both the forced one and the two bits related to the track indicator arriving from disk and then the whole content of MA is sent in the BU register and from here on the collector channel of CPU with the related accompanying trigger (TE20T).
The reading and sending to C.P.U. of the next two characters of the header takes place with the same procedures seen for the track header reading, as also the building -up and check of the cyclic code.
At the end of the header the SE counter advances of one position, the FF USBE and PELE are reset and the arrival of the configuration related to the next address mark is waited for.

6.2.6.3.6. Last header (ref. timing 78B103727page 18)

The last header reading occurs as the previous ones, except that with the TE20 accompanying the 36th character, the controller provides to send the signal of FINE to C.P.U., ending the transfer.
The controller stays still busy for the time necessary to end the checks on the cyclic code, then after it resets the FF LEGE, removes the read gate and provides to free itself.

6.2.6.3.7. Cases of end

The end is always issued by the controller in correspondence to the sending to C.P.U. of the 36th character.
It is not possible to read a length exceeding 36 characters or lengths which are not multiple of 3.
Generally either only the track header (6 characters)or the track header + the 10 headers (36 characters) are read.

6.2.6.3.8. Signals to the interface at the end of the command

CAPET : when the command has been rejected.

ERCAT : if a check error has occured on the command or a synchronization error on the characters exchanged.

SEGET : when a cyclic code error has occured on one or more headers read (FF ERCE = 1). It does not cause the instruction interruption.

PEOOT : it is absent from the moment in which the command arrives until the end of the cyclic code of the last header read.

MARET : when the end of track is reached without having completed the reading of the 10 written headers. This signal, which can be removed sending to the controller a general reset command 'para.6.2.5.1.) is generated in the following way :
at the beginning of the track to be read the FF RIDE is set, and if this one is still at 1,i.e. the read instruction is not yet completed at the arrival of the next index mark, with this same one the FF DIRO is set which sends the MARE signal towards the interface.

6.2.6.4. Headers verify (01001110)

6.2.6.4.1. General

The controller performs this particular type of instruction when, upon the reception of a verify command, the FF TETA is at logic 1.
With this instruction the characters sent by C.P.U. are compared bit by byt with the information that the head, previously selected, reads in the zones reserved to the headers.
This command behaves towards C.P.U.as a write command, towards the disc handler as a read command.
The header verify operation may be done only immediately after the writing of the headers themselves or,if applied after having written the field reserved to data,must be limited to the Track Header.
All the timings intervening in the check are derived from a delay line which cycles in synchronism with the information arriving from disk.
As these information might undergo frequency shifts,due to variatious in the disk speed both in the previous writing and in the deck under way,at the controller input there is an oscillator (P.L.O.)which modifies its frequency in function of the above mentioned variations and generates the pulses which will serve to the discriminator to form the gates suitable to divide the bits one from the clock bits.

As it was already seen previously at para. 6.1.11. if the discriminator outputs are not correct, the phase changing logic intervenes providing to make the ones (BILE) and the clocks (CCLE) come out on the correct lines.
The characters arriving from C.P.U. are put in the BU register and then subsequently in MA from where they are shifted at every delay line cycle.
The last FF of MA (MA07) is compared at proper times with the information arriving from disk and should a comparison error occur, the FF ERDA is set which will signal SEGET to the interface. The detection of an error does not fres the controller.
All the characters to be checked, except the first one, are asked in advance with respect to the transfer of the BU contents to MA as the C.P.U. will answer always with a certain delay with respect to the request.
The minimum time between TE1OT and TU2OT, acceptable by the controller is 1624 ns.
The counts of BI and subsequently those of DA are checked by the FF MOTO which, depending whether it is at logic 1 or 0, sets the counter BI to count in 8 or 6 bit mode.
The FF MOSE indicating the characters format must not have been set al logic 1 during the previous addressing.
The meaning of the various control FF which intervene in this instruction are:

USBI : at logic 1 it enables the outputs of the quartz oscillator and then the counts of BI and DA.

USBE : at logic 1 it enables the outputs of the delay line and then the counts of BI and DA.

RIGA : at logic 1 it gives the read "gate" to the unit.

GALE : at logic 1 it enables the outputs of the discriminator.

DUZE : at logic 1 it indicates that two characters zero have been recognized at the discriminator output and that therefore its output channels are correct.

ADMA : at logic 1 when the configuration related to the address mark has been recognised.

RICA : at logic 1 it enables the requests in cycle of the characters to be checked.

MOTO : at the logic 1 besides establishing the count mode of BI, it enables the shift of the MA register and detects the comparison period.

COCE : at logic 1 it enables the building-up of the cyclic code and the shift of the SH register.

6.2.6.4.2. Initial phase (ref. timing 78BI03727 page 6)

Upon the reception of the verify command, it is stored in the FF VERE; the FF SETE and DEME are set, which serve, the first one to start the head selection phase and the second the phase to wait for the track beginning.
Upon the index mark arrival, the counters BI and DA are reset and then the FF EDER is set which detects the zone concerning the Track Header and the FF USBI which starts the counts of the above mentioned counters.
With the decoding 5 of DA (DOO5) DEME is reset and with DO13, i.e. after about 60 us from the index mark, RIGA is set which provides to transmit to the unit the read gate.
At this point, the pulses sequence arriving to the controller provides to start the variable frequency oscillator (PLO), the discriminator and, if the outputs of this last one are inverted, the phase changing logic (refer to para. 6.1.11.).
The discriminator outputs are used only when the PLO is synchronized and, for this purpose, from the moment in which the read gate raises to when these outputs are used, a time equal to 7 characters must elapse.
With the decoding DO20 the configuration of the first 1 written on disk is forced in the counters BI and DA; the FF GALE is set which enables the discriminator outputs, the first character to be checked is requested and the recognition phase of two characters Zero on the discriminator data line starts.

6.2.6.4.3. Track Header (ref. timing 78BI03727 page 17)

After having recognized two characters (FF DUZE = 1), upon the arrival of the first bit on the data line, the FF USBE is set, which, for the whole period in which it stays at 1, allows the delay line to cycle and therefore

allows the output of all the timings necessary to the reading.
From the decoding D042 to D045, the FF RICA stays at 1 allowing the request in cycle of the characters; from the decoding D043 to D046, the FF MOTO stays at 1, allowing, at proper times the transfer from the register BU to the register MA of the three characters of the home address. At every cycle of the delay line, the content of MA is shifted and its last FF (MA07) is compared with the information arriving from disk (BADI) for the whole period of time in which MOTO stays set. In case of wrong comparison, FF ERDA is set.
The cyclic code is built-up on the information read making the Exclusive OR between every bit and the last FF of SH for the whole period in which the FF COCE stays at 1 and writing the result in the FF ORES and from here in the first FF of SH.
The contents of this register at the end of the 3 characters of the home address, if no errors have occured, are equal to the complement of the cyclic code, so continuing the operation of Exclusive OR at the end all FF of SH will be at one
If this condition is not verified, the FF ERCE is set and SEGET is signaled to the interface towards C.P.U.
With the decoding D070 the FF RICA raises and with D071 the FF MOTO, which stay at 1 respectively up to the decoding D073 and D074.
During this period of time, the characters related to the record zero are read and compared in the same way of the three previous characters.
After the cyclic code check, the register SE moves forward of one step, the FF USBE is reset and the address mark related to the 1st sector header is searched for.
The last character requested in this phase concerns the first character of the 1st sector header.

6.2.6.4.4. Header from the 1st to 9th sector (ref. timing 78B103727 page 18)

Once the address mark has been recognised (FF ADMA = logic 1)as described in para. 6.2.6.3.4. the pulse TIMA is generated which provides to ask for the 2nd character of the header and to transmit in the last two FF of the re-

gister MA the two less significant bits of BU, where there was stored the track indicator due to the arrival of the 1st character of the header requested in the previous phase.
At this point, the one-shot circuit P008 starts which, after having zeroed the counters BI and DA, at the end of its period (TAMA) forces at logic 1 the FF MOTO, PELE and RICA and in the above mentioned counters the configuration related to the first 1 of the subsequent "data mark".
Upon the arrival of the first 1 mentioned above, the FF USBE is set which, enabling the timings allows the shift of MA and then the check of the track indicator stored here with the one read from disk.
The check of the next two characters of the header occurs with the same procedures seen to check the track header and the building-up and check of the cyclic code.
After such a check, the counter SE moves forward of one step, the FF USBE and PELE are reset and the arrival of the configuration related to the next address mark is waited for.
The last request of this phase concerns the first character of the following header.

6.2.6.4.5. Last header (ref. timing 78B103727 page 18)

The check of the last header takes place as the previous ones, only that upon the arrival of the 36th character the controller provides to send to the CPU interface the signal of FINE and not to call for additional characters.
The controller stays still busy for the time necessary to end the checks on the cyclic code; after that it resets the FF VERE and removes the read gate and becomes free.

6.2.6.4.6. Cases of end

The end is always issued by the controller in correspondence to the arrival from C.P.U. of the 36th character.
It is not possible to check for a length exceeding 36 characters or for lengths which are not multiple of 3, otherwise there is the risk of not performing completely the comparison between the data sent from CPU and those read from disk.

6.2.6.4.7. Signal to the interface at the end of the command

CAPET : when the command has been rejected.

ERCAT : if a check error has occured on the command or a synchronism error on the characters exchanged.

SEGET : when a cyclic code error has occured in one or more headers read (FF ERCE = 1) or an error in the comparison among the data read and those arriving from C.P.U. (FF ERDA = 1). It does not interrupt the instruction under way.

PEOOT : it is absent from the moment in which the command arrives to the end of the cyclic code of the last header read.

MARET : when the track end is reached without having finished the reading of the 10 headers written. This signal, which can be eliminated sending to the controller a general reset command, is generated in the following way:
at the beginning of the track to be checked the FF RIDE is set and if this is still at 1, i.e. the read instruction has not yet been completed at the arrival of the next index mark, with that same one the FF DIRO is set which causes the signal MARE to the interface.

6.2.6.5. Data writing (01000010)

6.2.6.5.1. General

The controller performs this special type of instruction when, upon reception of a write command, the FF TETA is at logic 0.
With this instruction the head previously selected writes on disk, in the field, reserved to the data, related to the addressed header, the serialized information derived from those transmitted from C.P.U.
The timings needed during the writing phase are derived by a quartz oscillator which oscillates at the frequency of 2.5 MHz while those which intervene during the phase

to recognize the header are derived from a delay line which performs its cycle in synchronism with the information arriving from disk.
Every cell of the pulses sequence written on disk is always formed by a bit followed after 400 ns by its clock.
The characters to be recorded are stored in the register BU and from here they are transferred in the register MA when the following character has already been requested, as the CPU will answer always with a certain delay with respect to the request.
The minimum time between TE10T and TU20T, acceptable by the controller is 1684 ns.
This instruction has the capacity to work with the TE30 set at logic"1",in fact when the controller gives to CPU the signal of having received the first character transmitted, the FF TEMA is set which maintains at logic one the TE30 for all the period of the transfer.
The purpose of the TE30 at logic one is the one to reduce to 0 the delay between TU20T accompanying the character and the TE30T indicating that the character has been received.
The request of the first character is done long before the following ones, which are in cycle.
The maximum capacity of every block is of 288 characters if the characters format is at 8 bit mode (MOSE = 0) or 384 characters if instead it is at 6 bit mode (MOSE = 1).
The FF MOTO in AND with MOSE times the counts of the counters BI and then DA.
In the 8-bit mode writing of data all the bits of each character sent from CPU are written unchanged, in the 6-bit mode the first 6 bits of every character are written unchanged and bits b_7 and b_8 are ignored.

In the 6-bit mode writing no error synchronism check is performed. The FF which intervene to check the performance of this instruction are the same ones seen for the headers writing described in para. 6.2.6.2.1.

6.2.6.5.2. Initial phase (ref.timing78B103727 page 6)

In this phase which is common to all the operations on data, when the write command is received, it is stored in the FF REGE (in the FF LEGE in case of reading and VERE in case of verify),then the FF SETE and RITA are set which

serve, the first one to start the head selection phase by sending to the disk unit the BUS5U bus line accompanied by the tag control SERIU and the second to enable the search for the addressed header.
At this point a period of time of about 60 μs must elapse, necessary for the head selection, setting the FF USBI which starts the counts of BI and DA and waiting for the decoding D013 of this last one. The FF RIGA is set which through the BUS1U bus line gives the read gate to the unit.
With the decoding DC20 of DA, after the PLO has synchronized, the discriminator outputs are enabled setting the FF GALE.
Now the two characters zero (DUZE = 1) must be recognized and then the phase is started to search for the configuration related to the first address mark which is met, as described in para. 6.2.6.3.4.

6.2.6.5.3. Search for the beginning header (ref. timing 78B103727 page 16-19)

Once the address mark has been recognized (FF ADMA = logic 1) as described in para. 6.2.6.3.4., it makes the one-shot circuit F008 start which after having zeroed the counters B1 and DA, at the end of its period generates the pulse TAMA which forces at logic 1 the FF MOTO and PELE and in the above mentioned counters the configuration related to the first 1 of the subsequent "data mark".
In addition TAMA writes in the last two FF of the register MA the contents of the register TI concerning the track indicator stored in it with the addressing command.
At the arrival of the first 1 of the "data mark" the FF USBE is set which, enabling the timings (TI00 - TI03) allows the shift of MA and therefore the check bit by bit that the track indicator read from disk is equal to the one stored.
The same operation of storage in MA and of check is repeated both for the information related to the cylinder stored in the register CI and the one of the head and of the sector stored respectively in HE and SE.
The cyclic code which must be equal to the one written after the header itself is built up on the bits related to the header under exam.

If the header read is equal to the one addressed by the TI, CI, HE and SE registers and the related cyclic code is correct, the FF COCE, RITA, RICA, USBE are reset and the operations are started on the data setting the FF DATI. In addition, the counter SE counts +1 so its FF assume the configuration related to the subsequent sector address, allowing in this way the search for the next header when the length of the block on which to operate exceeds the maximum capacity of the data field of a sector.
At the end of this phase, the FF NOTE and TIDI must be at logic zero.

6.2.6.5.4. Executive phase of writing (ref. timing 78B103727 page 20)

Once the header has been recognized, the counts of BI and DA which in the previous phase were enabled by the FF USBE go on without interruption with the pulses of the quartz oscillator enabled by the FF USBI.
Therefore the FF GAPE is set at logic 1 and with decoding D023 the FF DIGA and ERAS are set which serve respectively to transmit to the selected unit the write gate on the BUSOU line and the erase gate on the BUS4U bus line.
Now 12 zero characters are written, from decoding D023 to D035, then GAPE is reset.
The out-of-cycle request of the first character to be written in the field reserved to data was done with D031 and then in transmitting to C.P.U. the signal of reception of the requested character the FF TEMA was set which has the purpose to keep at logic one the TE30 for the whole period of transmission.
Then 6 bits one are written and right after that, the configuration related to the "data mark".
The FF RICA is set with the decoding D036 and the FF MOTO is set with the decoding D037, which serve respectively, the first one, to enable the request of characters in cycle and the second, besides establishing in AND with MOSE the count mode of BI, to establish the transfer of the contents of the BU register in MA and then the shift of this last one.
The FF MOTO in AND with COCE enables the building up of the cyclic code through the FF ORES and the SH register as already seen in para. 6.2.6.2.3.

Depending whether the characters format is 8-bit mode or 6-bit mode, the data field may be of 288 or 384 characters so RICA remains at logic 1 up to the decoding 324 or 420 of DA (T324), the FF MOTO up to the decoding 325 or 421 (T325) and the FF COCE up to the decoding 327 or 423 (T327). If MOSE is at 1 the FF OSEI follows the FF MOTO and makes BI count in 6-bit mode in the data field. The FF CHEC as usual allows the writing on disk of the cyclic code related to the whole block; then the "post data" is written, the FF DIGA is reset and, after 10 counts of DA, the FF ERAS.
At this point, the head selection is removed if it is the last sector of a track and the operation must continue on the subsequent or the signal of end from C.P.U.(FINUT) has arrived.
In the 2nd case, the pulse RESE is generated which resets the FF which at the end are at logic 1 and frees the controller.

6.2.6.5.5. Passage from one sector to the following (ref. timing 78B103727page 20)

This case occurs every time that blocks exceeding the maximum capacity of a sector data field must be written and therefore the operation started on a sector does not end at the end of the sector itself, but continues on the subsequent one within the same track.
The writing of the first sector occurs as described sub para. 6.2.6.5.4. then, if the operation must continue, with the decoding T342 the FF RIGA is set which sends the read gate to the selected unit, with the same procedures the FF GALE is set which enables the discriminator outputs, two characters zero are recognized (FF DUZE = logic 1) and the configuration related to the "address mark" of the next header is waited for a described in para. 6.2.6.5.3.
If this last one will be recognized as being equal to the contents of registers TI, CI, HE and SE the remaining characters will be written as described in para. 6.2.6.5.4.

6.2.6.5.6. Passage from one track to the subsequent (ref. timing 78B103727 page 20)

This case occurs every time the writing has been started on a track and must continue on the subsequent track within the same cylinder.
The writing of the last sector of the track occurs as described sub para. 6.2.6.5.4. then if the operation must continue on the first sector of the subsequent track, the head selection is removed resetting the FF SETE and the BUS7U (EDVA) bus line is sent to the unit followed after a certain time by the tag control (ADVA) in order to make count +1, both the counter which on the disk handler stores the head code and the one on the controller (HE).
Upon the arrival of the index mark, the selection is sent to the new head setting again the FF SETE and after having performed the phase described in para. 6.2.6.5.2. the subsequent header is searched for.

6.2.6.5.7. Last sector of a cylinder (ref. timing 78B103727 page 20)

If a writing is under way on the last sector of a track and, at the end of the sector itself, the transfer is not over yet, the controller behaves as per para. 6.2.6.5.6., except that, if the track is the last one of a cylinder, the disk handler sends to controller the signal of cylinder end (FICIU).
This signal, which has been caused by the fact that the counter, storing the head code on the unit, has counted +1, is stored on the controller in the FF FISE at the subsequent index mark and it is transmitted to C.P.U. on the lead which signals end of sequence (FISET).
Meanwhile, the FF ERPO is set, a character is requested from C.P.U. and upon its arrival the end from controller (FINET) is signaled to C.P.U.
With the subsequent TU20.FINU, the controller is freed.
In this case a character exceeding those actually written in disk is exchanged with C.P.U.

6.2.6.5.8. Last sector of alternative track

If a writing is under way on the last sector of an alternative track and at the end of the track itself the transfer has not yet been completed, the controller behaves as per para. 6.2.6.5.6. setting also the FF FIPI which is sent in OR by the signal of cylinder end sent by the disk handler, so the controller behavior is similar to the one described in para. 6.2.6.5.7.
At the end of the instruction, the signals of sequence end (FISET) and end from outside (FINET) are sent to C.P.U.

6.2.6.5.9. Checks

During the performance of this instruction, the following checks are made:

- consecutiveness check between the header of a sector and the subsequent one (refer to para. 6.2.6.9.1.);
- check that the head-holding arm is positioned on the addressed track (refer to para. 6.2.6.9.2.);
- check that the track indicator read is equal to the one addressed (refer to para. 6.2.6.9.3.).

6.2.6.5.10. Cases of end

a. End from C.P.U.

If the end is issued from C.P.U. when the last sector interested to the instruction has not yet been completed, the controller provides to stop the characters request (TEIOT) and to write "0" until the sector is completed.
During this time, both the controller and the disk handler stay busy.

b. End from controller.

The controller provides to signal the end (FINET) to C.P.U. in the following cases:

- when at the end of the writing of the last sector of a cylinder, the transfer has not yet been completed (para. 6.2.6.5.7.), also the cylinder end (FISET) is signaled;
- when at the end of the writing of the last sector of an alternative track, the transfer has not yet been completed (para. 6.2.6.5.8.), also the cylinder end (FISET) is signaled;
- when a consecutiveness error occurs on the headers (para. 6.2.6.9.1.), also EGOLT is signaled;
- when, because of a wrong positioning, the beginning header cannot be found within a certain time (para. 6.2.6.9.2.), also EGOLT is signaled;
- when a track indicator different from the one addressed has been detected (para. 6.2.6.9.3.), both EGOLT and IGOLT are signaled.

In all the cases listed above, the controller exchanges with C.P.U. a character more than those actually written on disk.

6.2.6.6. Read Data (01000000)

6.2.6.6.1. General

The controller performs this special type of instruction when, upon reception of a read command, the FF TETA is at logic 0.
In this instruction the head previously selected, after having found the addressed header, transfers the serialized information of the subsequent data field from the disk handler to the controller which, after having parallelized them, sends them to C.P.U. with the related accompanying trigger.
The timings which intervene are derived from a delay line which cycles in synchronism with the information arriving from disk.
The procedures to read and transfer the information to C.P.U. are the same ones seen for the headers reading (para. 6.2.6.3.1.).

The data block consists of 2304 bits, which may be read in 8-bit mode (288 characters) or in 6-bit mode (384 characters) depending whether the FF MOSE is at logic "0" or "1".
As we have seen previously, the FF MOSE and MOTO drive the counts of BI and DA.
In the 8-bit mode, the bits read are sent unchanged to C.P.U., while in the 6-bit mode, the controller provides to re-build the information to 8 bits to send it to the interface, expanding the information in the following way: the first 6 bits (AIFUT - FIFUT) stay unchanged while the 7th bit is equal to the complement of the 6th bit (GIFUT = $\overline{\text{FIFUT}}$) and the 8th bit is equal to the 6th (LIFUT = FIFUT).
In the 6-bit mode reading, the synchronization check is not performed.

6.2.6.6.2. Initial phase and beginning header search

(ref. timing78B103727 page 6-16-19)

The initial phase and the one of the beginning header phase are similar to the write phase described in para. 6.2.6.5.2. and 6.2.6.5.3.

6.2.6.6.3. Reading execution phase (ref. timing78B103727 page 21)

Once the header has been recognized, the counts of BI and DA, which in the previous phase were enabled by the FF USBE, go on without interruption with the pulses of the quartz oscillator enabled by the FF USBI.
The possible splice area must be overcome which might exist between the 10 characters of the "Erase delay" and the 12 characters zero which from time to time are written in the data writing operations and which is almost coincident with the decoding D023 of DA.
With the decoding D025 the FF PELE is set and the read gate is sent again to the unit (FF RIGA = logic 1).
With the decoding D031 the FF USBI is reset, the PLO outputs are enabled setting the FF CALE and the configuration of the first "one" written on disk (F035) is forced in counters BI and DA.

Once two characters zero (DUZE = 1) have been recognized at the arrival of the above mentioned "one" from disk (DALE), the FF USBE is set, which enables again the timings in synchronism with the disk.

With the decoding D037 which detects the data field beginning, the FF MOTO is set which enables the loading of the MA register with the information arriving from disk and, at the end of every character, the character transfer to C.P.U.

If MOSE is at 1, the FF OSEI follows the FF MOTO and makes BI count in 6-bit mode and allows the transfer in BU of only the first 6 bits of MA.

The transfer of the MA contents in BU is done by the pulse MABU which provides also to generate the character accompanying trigger towards C.P.U. (TE2OT).

At the decoding D037 also the FF COCE raises which enables, for the whole period in which it stays at 1, the building-up of the data field cyclic code allowing the Exclusive OR between the bits of the information read and the contents of the last FF of SH. The result of the above mentioned operation is stored every time in the FF ORES and from here in the 1st FF of SH.

At the end of the block, the contents of the register SH must be equal to the complement of the cyclic code, so continuing the operation of Exclusive OR at the end all FF of SH will be at one.

If this condition is not verified, the FF ERCE is set and SEGET is signaled to the interface towards C.P.U.

With the decoding T325 the FF MOTO is reset and with the decoding T327 the FF COCE and USBE are reset while the FF USBI is set.

With the decoding T338 the head selection is removed if it is the last sector of a track and the operation must continue on the following, or the signal of end from C.P.U. (FINUT) has arrived.

In the 2nd case the pulse RESE is generated which resets the FF which at the end are at logic 1 and frees the controller.

6.2.6.6.4. Passage from one sector to the subsequent

(ref. timing 78B103727 page 21)

This case occurs when the block to be read exceeds the maximum capacity of a sector data field and therefore the operation will have to continue on the following sector within the same track.
The reading of the first sector takes place as described in para. 6.2.6.6.3., then, if the operation must continue up to the decoding T342, the FF RIGA is set and sends the read gate to the selected unit, with T348, the FF GALE is set and enables the discriminator outputs.
Then two zero characters are recognized (FF DUZE = logic 1) and the configuration related to the "address mark" of the next header is waited for as described in para. 6.2.6.5.3.
If this last one will be recognized as equal to the contents of the register TI, CI, HE and SE the remaining characters will be read as described in para. 6.2.6.6.3.

6.2.6.6.5. Passage from one track to the subsequent one

(ref. timing 78B103727 page 21)

This case occurs every time that the reading has been started on one track and must continue on the subsequent track within the same cylinder.
The reading of the last sector of a track occurs as described in para. 6.2.6.6.3. then, if the operation must continue on the first sector of the subsequent track, the head selection is removed resetting the FF SETE and the BUS7U bus line (EDVA) is sent to the unit followed after a certain period of time by the tag control (ADVA) so that both the counter that on the disk handler stores the head code and the one on the controller (HE) count +1.
At the arrival of the index mark the selection is sent to the new head setting again the FF SETE and, after having performed the phase described in para. 6.2.6.5.2., the subsequent header is looked for.

6.2.6.6.6. Last sector of a cylinder (ref. timing 78B103727page 21)

If a reading is under way on the last sector of a track and, at the end of the sector itself, the transfer has not yet been completed, the controller behaves as per para. 6.2.6.6.5. except that, if the track is the last one of a cylinder, the disk handler sends to the controller the end of a cylinder signal (FICIU).
At the subsequent index mark this signal is stored in the FF FISE and transmitted to CPU on the lead signaling end of sequence (FISET); in the same instant the FF ERPO is set and the signal of end from outside (FINET) is transmitted to CPU with the related accompanying trigger (TE20).
When the C.P.U. will send the end (FINUT), on the controller the pulse RESE shows which will provide to reset the main FF of the controller and to free it.
In this case the controller exchanges a spurious character with CPU.

6.2.6.6.7. Last sector of alternative track

If a reading is under way on the last sector of an alternative track and at the end of the track itself, the transfer has not yet been completed, the controller behaves as per para. 6.2.6.6.5. setting though also the FF FIPI which is sent in OR with the signal of cylinder end sent by the disk handler, so the controller behavior is similar to the one described in para. 6.2.6.6.6.
The signals sent to CPU are those of end of sequence (FISET) and of end from ourside (FINET).

6.2.6.6.8. Checks

During the performance of this instruction, the following checks are applied:

- consecutiveness check between the header of a sector and the one of the subsequent (refer to para. 6.2.6.9.1.);
- check that the head-holding arm is positioned on the addressed track (refer to para. 6.2.6.9.2.);

- check that the track indicator read is equal to the addressed one (refer to para. 6.2.6.9.3.).

6.2.6.6.9. Cases of end

a. End from C.P.U.

If the end is issued by C.P.U. when the last sector interested by the instruction has not yet been completed, the controller provides to stop the transfer of the characters to C.P.U., but it completes the reading of the whole sector and checks the correctness of the cyclic code.
During this period both the controller and the disk handler are busy.

b. End from controller.

The controller provides to signal the end (FINET) to CPU in the following cases:

- when at the end of the reading of the last sector of a cylinder the transfer has not yet been completed (para. 6.2.6.6.6.), also the end of cylinder (FISET) is signaled;
- when at the end of the reading of the last sector of an alternative track the transfer has not yet been completed (para. 6.2.6.6.7.), also the end of cylinder (FISET) is signaled;
- when a consecutiveness error occurs on the headers (para. 6.2.6.9.1.), also EGOLT is signaled;
- when because of a wrong positioning the beginning header cannot be found within a certain period of time (para. 6.2.6.9.2.), also EGOLT is signaled;
- when a track indicator different from the addressed one has been detected (para. 6.2.6.9.3.), both EGOLT and IGOLT are signaled.

In all the above listed cases, the controller exchanges a spurious character with CPU.

6.2.6.7. Initialization reading

6.2.6.7.1. General

The controller performs this special type of instruction when, after having received from GPU the signal of general reset (CAGUT), the C.P.U. itself sends it a read command.
The reset signal had put to logic zero the FF TETA and MOSE and to logic 1 the FF LEIN forcing the addressing registers of the controller in order to address the sector "0" of the track "0" of the cylinder 00 with the track indicator set to indicate good track.
This instruction is performed in all its phases as a normal data reading (para. 6.2.6.6.) except that here the FF SINO intervenes which allows to send to CPU the even characters written on disk.
At the end of the 2nd sector and in correspondence of the TE20 accompanying the last character, the controller sends to CPU the signal of end from outside (FINET) and with the subsequent FINUT the controller is freed.

6.2.6.8. Data Verify (01001110)

6.2.6.8.1. General

The controller performs this special type of instruction when, upon the reception of a verify command, the FF TETA is at logic 0. In this instruction the head previously selected, after having found the addressed header, transfers the serialized information of the subsequent data field, from the disk handler to controller where they are compared bit by bit with the characters sent from C.P.U.
As far as this last one is concerned, the check command behaves as a write command while, as far as the handler is concerned, it behaves as a read command.
All the timings which intervene in the execution phase of the check are derived from a delay line which cycles in synchronism with the information arriving from disk.

The procedure to read from disk and compare with the information arriving from CPU are the same as those seen for the headers check (para. 6.2.6.4.)

This instruction has the peculiarity to work with the TE30 set at logic one so to reduce to zero the echo time between the TE20T accompanying the character to be compared and its TE30T indicating reception.

In the TE30 indicating the reception of the first character, which is requested in advance with respect to the following ones which are in cycle, the FF TEMA is set which maintains at logic one the TE30 for the whole period of the transfer.

As we have already seen previously, the FF MOTO and MOSE adjust the counts of BI and DA.

If the contents of a whole block are checked and operation is in 8-bit mode, the characters exchanged with C.P.U. are 288; if operation is in 6-bit mode they are 384; in the first case the FF MOSE is at logic zero, in the second it is at logic 1.

In the 6-bit mode, the bits b_7 and b_8 of every character arriving from CPU are not compared and the synchronism check is not performed.

6.2.6.8.2. Initial phase and beginning header search

(ref. timing 78B103727 page 6-16-19)

The initial and the beginning header search phase are similar to the one for writing described in para. 6.2.6.5.2. and 6.2.6.5.3.

6.2.6.8.3. Check execution phase (ref. timing 78B103727 page 22)

Once the header has been recognized, the counts of BI and DA, which in the previous phase were enabled by FF USBE, go on without stopping with the quartz oscillator pulses enabled by FF USBI.

A way is found to overcome a possible splice area existing between the 10 characters of the "Erase delay" and the 12 characters zero which from time to time are re-written in the data writing operations and which is almost coincident with the decoding D023 of DA.

With the decoding D025 the FF PELE is set and the read

gate is sent again to the unit (FF RIGA = logic 1).
With decoding D031 the FF USBI is reset, the PLO outputs are enabled and the pulse FODA is generated, which has the purpose to force in the counters BI and DA the configuration of the first one written on disk and to generate the request of the first character to be compared to C.P.U.
With the TE30 indicating the reception of this character, the FF TEMA is set on the controller which will maintain at logic one the TE30 up to the end of the transfer.
Once two characters zero have been recognized (DUZE = 1), upon the arrival of the first bit one from disk the FF USBE is set which enables again the timing in synchronism with the disk.
With decoding D036 the FF RICA is set which enables the requests of the characters in cycle to C.P.U.; with decoding D037 both the FF CODA and the FF MOTO are set which respectively serve, the first one to enable the comparison bit by bit of the information and the second, beside establishing in AND with MOSE the count mode for BI, to enable the transfer of the contents of the register BU in MA and consequently the shift of this last one.
If MOSE is at 1, the FF OSEI follows the FF MOTO and makes BI count in 6-bit mode and allows to take out from the comparison the last two bits of every character stored in MA (MA06 and MA07).
With a certain advance with respect to the transfer of the contents of BU in MA the subsequent characters to be compared with C.P.U. are requested.
With decoding D037 also the FF COCE has raised which enables, for all the period in which it remains at 1, the building up of the cyclic code of the data field, allowing the Exclusive OR between the bits of the information read and the contents of the last FF of SH.
The result of the operation mentioned above is stored, from time to time in the FF ORES and from here in the first FF of SH.
At the end of the block, the contents of the SH register must be equal to the complement of the cyclic code, so continuing the operation of Exclusive OR at the end all FF of SH will be at one.
If this condition is not verified, the FF ERCE is set and SEGET is signaled to the interface towards CPU.
With decoding T325 theFF MOTO and CODA are reset and with decoding T327 the FF COCE and USBE are reset while

the FF USBI is set.
With decoding T338 the head selection is removed if it is the last sector of a track and the operation must continue on the subsequent one, or the signal of end from C.P.U. (FINIT) has arrived.
In the second case the pulse RESE is generated which resets the FF which at the end are at logic 1 and frees the controller.

6.2.6.8.4. Passage from one sector to the following

(ref. timing 78B103727 page 22).

This case occurs when the block to be checked has a length exceeding the maximum length of the data field of a sector and therefore the operation will have to continue on the following sector within the same track.
The check of the first sector occurs as described sub para. 6.2.6.8.3. then, if the operation must continue up to decoding T342, the FF RIGA is set which sends the read gate to the selected unit; with T342, the FF GALE is set which enables the discriminator outputs.
Then two characters zero (DUZE = logic 1) are recognized and the configuration related to the "address mark" of the next header as described in para. 6.2.6.5.3. is waited for.
If this last one will be recognized equal to the contents of the registers TI, CI, HE and SE, the remaining characters will be read as described in para. 6.2.6.8.3.

6.2.6.8.5. Passage from one track to the following

(ref. timing 78B103727 page 22).

This case occurs every time that the check has been started on one track and it must continue on the subsequent track within the same cylinder.
The check of the last sector of a track occurs as described sub para. 6.2.6.8.3. then if the operation must continue on the first sector of the subsequent track, the head selection is removed resetting the FF SETE and the bus line BUS7U (EDVA) is sent to the unit followed after a certain period of time by the tag control (ADVA) so to

make count +1 both the counter which on the disk handler stores the head code and the one on the controller.
At the arrival of the index mark the selection is sent to the new head setting again the FF SETE and after having performed the phase described in para. 6.2.6.5.2. the following header is looked for.

6.2.6.8.6. Last sector of a cylinder (ref. timing 78B103727 page 22)

If a check of the last track sector is under way and, at the end of the sector itself, the operation has not yet been completed, the controller behaves as per para. 6.2.6.8.5. except that if the track is the last one of a cylinder, the disk handler sends to the controller the signal of cylinder end (FICIU).
This signal, caused by the fact that the counter storing the head code on the unit has counted +1, is stored in the FF FISE and at the following index mark sent to CPU on the lead signaling end of sequence (FISET).
Meanwhile the FF ERPO is set, a character is requested to CPU and upon its arrival, the end from controller (FINET) is signaled to CPU.
With the subsequent TU20.FINU the controller becomes free. In this case a spurious character is exchanged with C.P.U.

6.2.6.8.7. Last sector of alternative track

If a check of the last sector of an alternative track is under way, and at the end of the track itself the transfer has not yet been completed, the controller behaves as per para. 6.2.6.8.5. setting,though,also the FF FIPI which is sent in OR with the signal of end of cylinder sent by the disk handler, so the behavior of the controller is similar to the one described in para. 6.2.6.8.6.
The signals sent to CPU are those of end of sequence (FISET) and of end from outside (FINET).

6.2.6.8.8. Checks

During the performance of this instruction, the following checks are made:

- check the consecutiveness between the header of one sector and the following one (refer to para. 6.2.6.9.1.);
- check that the head-holding arm is positioned on the addressed track (refer to para. 6.2.6.9.2.);
- check that the track indicator read is equal to the addressed one (refer to para. 6.2.6.9.3.).

6.2.6.8.9. Cases of end

a. End from C.P.U.

If the end has been issued by C.P.U. when the comparison of the last sector interested by the instruction has not yet been completed, the controller provides to stop both the request of characters to CPU and the data comparison.
The reading continues until the whole sector is completed in order to verify the correctness of the cyclic code.
During this time, both the controller and the disk handler stay busy.

b. End from controller.

The controller provides to signal the end (FINET) to CPU in the following cases:

- when at the end of the check of a cylinder last sector, the transfer has not yet been completed (para. 6.2.6.8.6.), also the end of cylinder (FISET) is signaled;
- when at the end of the check of the last sector of an alternative track the transfer has not yet been completed (para. 6.2.6.8.7.) also end of cylinder (FISET) is signaled;
- when a consecutiveness error occurs on the headers (para. 6.2.6.9.1.), also EGOLT is signaled;

- when because of a wrong positioning the beginning header cannot be found within a certain time (para. 6.2.6.9.2.) also EGOLT is signaled;
- when a track indicator different from the addressed one has been detected (para. 6.2.6.9.3.) both EGOLT and IGOLT are signaled.

In all the cases mentioned above, the controller exchanges one character more with CPU.

6.2.6.9. Checks during the operations on data

6.2.6.9.1. Consecutiveness checks

This is a check which intervenes every time the operation started on one sector must continue on the subsequent sector within the same track or cylinder and it is done in the following way: when the beginning header is recognized, the FF RICO is set and if the following headers are not consecutive to the first one, both the FF EGOL which transmits the EGOLT signal to the CPU interface and the FF ERPO are set on the controller.
At this point two cases can be distinguished:

a. Write and verify.
If a data write or verify operation is under way, when FF ERPO raises a character is requested from CPU (TE 1OT); upon the arrival of this character, the controller sends to CPU the signal of end from the outside (FINET)and at the signal FINUT of answer it becomes free. In this case a character more than those written on disk is exchanged.

b. Read.
If a read operation is under way when FF ERPO raises, also the FF FINE raises which transmits to the interface the signal of end from outside (FINET) and the trigger accompanying the signal itself (TE2OT) is generated.
The controller, which in this case exchanges a spurious character with CPU becomes free when the CPU sends the signal of end (FINUT).

In order that this control does not give error, the headers must be written as indicated in para. 4.3.4.

6.2.6.9.2. Positioning check

This check intervenes if the beginning header is not found within two consecutive "index marks".
When searching for the header, upon the arrival of the first "index mark" the FF RIDE is set and it is reset when the beginning header is found; if this has not yet occured upon the arrival of the second index mark both FF EGOL, which transmits to the CPU interface the EGOLT signal, and the FF ERPO are set.
At this point the cases described sub points a. and b. of para. 6.2.6.9.1. can be distinguished.
This check is performed also in the passage from one track to the subsequent.

6.2.6.9.3. Track indicator check

If in the phase to search for the header the track indicator of the header read is different from the one stored in the TI register, the FF TIDI is set which is reset at the end of the check of the header cyclic code, if this is wrong or it stays at logic 1 signaling IGOLT to the CPU interface, if it is correct.
If the beginning header is not found within two subsequent "index marks" the EGOLT signal shows as described in para. 6.2.6.9.2. which will be present together with IGOLT.
At this point the cases described sub points a) and b) of para. 6.2.6.9.1. can be distinguished.

6.2.7. Logic for the diagnostics

6.2.7.1. General

This logic essentially consists of a counter which counts +1 every time the CPU sends to the controller a command of selector advance.
The decodings of the FF counter have the task to start some special logics which allow to simplify the controller diagnosis.

6.2.7.2. Selector advance command

This command, which must be used only by the diagnostics, is done by the controller every time,in the information arriving from CPU related to the command code,there are either bit EIFUT or bit LIFUT.
These two signals, which are derived directly from the interface receivers,are set in OR between them and subsequently pulsed by the signal TUDI derived by the pulse accompanying the command itself (TU2OT).
The controller never rejects this command, even if at the end of the command itself there is on the CPU interface the signal CAPET.

6.2.7.3. Position 00

The diagnostic position 00 is determined by the decoding OODI of the FE counter; after a clear, it is set in position 00.
This position enables the sending of the signal of end (FINET) to CPU; in positions different from 00 the end is stopped.

6.2.7.4. Position 01

The diagnostics position 01 is determined by the decoding 01DI of the counter FE.
In this position the controller behaves in the following way:

- it inverts the check bit of the information arriving from the distributor channel, exchanging between them the normal conditions of set and of reset of FF BU08 of the BU register, where the signal MIFUT should be stored.

6.2.7.5. Position 02

The diagnostic position 02 is determined by the decoding 02DI of the counter FE.
In this position, the controller behaves in the following way:

- upon the reception of an header writing command it writes in the wrong way all the cyclic codes related to the headers themselves (either all "1" or all "0");
- upon the reception of an end command (FINUT) from C.P.U. during a writing, reading or check with the reset of the FF MOTO, the status of SH related to the cyclic code of the information read or to be written is frozen.
  The contents of SH may be seen analyzing the signal NOZE connected on the lead NU1OT of the interface with CPU;
- it stops the issue of the signal TIBI which when COCE is going down would reset the register SH;
- it stops the synchronism check causing then the raise of the error channel signal (ERCAT).

6.2.7.6. Position 03

The diagnostic 03 position is determined by the decoding 03DI of the counter FE.
In this position, the controller behaves in the following way:

- it stores the signal PORI in the FF FISE
- it stores the signal POTI in the FF 08RI
- it stores the signal POLI in the FF 09RI
- it stores the signal PORE in the FF ERDA

The contents of these FF may be pseudoread in the diagnostic position 10.

6.2.7.7. Position 00 - 03

The diagnostic positions from 00 to 03 are determined by the signal ABER.
When ABER is at logic 1, the outputs of the register BU are connected to the collector channel of CPU and the raise of the improbability signal (CAPET) is enabled.
When ABER is at logic 0, the normal ways to generate the TE20 accompanying the character are stopped and the same ones are generated inconditionally at every request of the CPU (TU1OT); also tho switching of the FF GIRO is enabled.

For the whole period in which ABER is at zero, the pseudo reading of the signals internal to the controller connected with the collector channel are performed.

6.2.7.8. Position 04 - 10

These positions are determined by the decodings from 04DI to 10DI of the counter FE; each one of the positions enables to send to the CPU collector channel some signals internal to the controller allowing their reading.
The table below gives the internal signals which at every diagnostic position are sent to CPU on the various leads of the collector channel:

	AIFE	BIFE	CIFE	DIFE	EIFE	FIFE	GIFE	LIFE
ABER	BU00	BU01	BU02	BU03	BU04	BU05	BU06	BU07
04DI	0837	4371	4674	4876	T325	T378	T323	0535
05DI	4573	T324	T342	4819	T338	1336	D031	D374
06DI	ABU0	ABU1	DEME	ORTA	ABU4	ABU5	USBI	GIRO
07DI	OTTO	EDER	TRAC	COCE	GAPE	CHEC	RICA	GIRO
08DI	PELE	USBE	08RI	GALEN	GAINN	MISI	DATI	GIRO
09DI	CODIN	NOTE	RITA	RIDE	APLO	DUZE	ADMA	GIRO
10DI	FIPIN	PIRI	TEST	09RI	TEMA	09HE	02SE	00SE

6.2.7.9. Position 11

The diagnostic position 11 is determined by the decoding 11DI of the counter FE.
In this position, upon the reception of an header writing command, the clock writing in the zone of the "missing clocks" does not stop.

6.2.7.10. Signals sent on free interface leads

The interface leads not used by the controller are used to send to CPU some internal signals as indicated below:

Internal signal	Interface signal
ORIUN	MAPET
O4TE	MATET
NOZE	NU1OT
OODI	NU2CT
OOBI	NU3OT

6.2..7.11. DA counter test

There is the possibility to make the DA character counter count step by step sending to the controller an addressing or positioning command when the diagnostics selector is in positions 04 or 05 and then pseudoread the counter contents.
The counts are in relation with the number of characters sent with the above mentioned commands.
The counter contents may be pseudoread in position 04 and 05.

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ALI 130/B

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PRODUCT DESIGN SPECIFICATIONS

ALI 130/B - POWER SUPPLY

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1. GENERAL CHARACTERISTICS

1.1. Electric characteristics

INPUT

Three-phase power supply voltage	V eff.	220 o 208
Power supply voltage frequency	Hz	50 o 60
Absorbed power with full load	V A	660
Current absorbed by phase at full load	A eff. **	
Power factor with full load	cos	0,87
Yeld		0,433

OUTPUT

Continuous nominal voltage	V	+3	-3	+5,2	+5,2	-36
Continuous nominal current	A	3,2	8,24	12	15,5	2
Max. Error on the output voltage	%	2	2	3	3	3
Max. Error in static regim	mV	10	30	140	160	90
Max. Error in dynamic regime	mV	10	10	50	50	50
Time needed to return within the adjustment range for dynamic variations	mS	20	20	50	50	50
Ripple	mV	15	15	40	40	40
Maximum performance temperature limits	°C	+ 10 + 38				
Thermal shift	mV/°C	1,5	0,4	4,5	5,4	15
Developed Kcal/h	280					

* As it a power supply with three-phase and mono-phase supply, the absorptions on the single phases are:

Phase	X	2.3	A
	Y	2.1	A
	Z	1.25	A

1.2. Introduction

The ALI 130 supplies the d.c. power supply voltages to the DSC 157 subsystem

It supplies the following stabilized voltages:

-36	V	with a maximum current of	2	A
-3	V	with a maximum current of	8.24	A
+3	V	with a maximum current of	3.2	A
+5	V	with a maximum current of	12	A
+5	V	with a maximum current of	15.5	A

The voltages -36V, +5V, were obtained by means of a "Switching" adjustment system.
In order to reoover the voltage failures on the distribution cables the output voltage of the +5V boxes must be adjusted to 5.2V.
The +3V voltage was obtained by means of a parallel adjustment system.
The -3V voltage was obtained by means of a mixed system of SCR pre-adjustment and parallel adjustment.

1.3. Physical configuration

The power supply consists of 2 and a half SMN modules labeled as follows:

Transformers module (1 module), Adjustments module (1 module), Commands module (½ module) Fig. 1 - 1.

Weight Kg. 70.

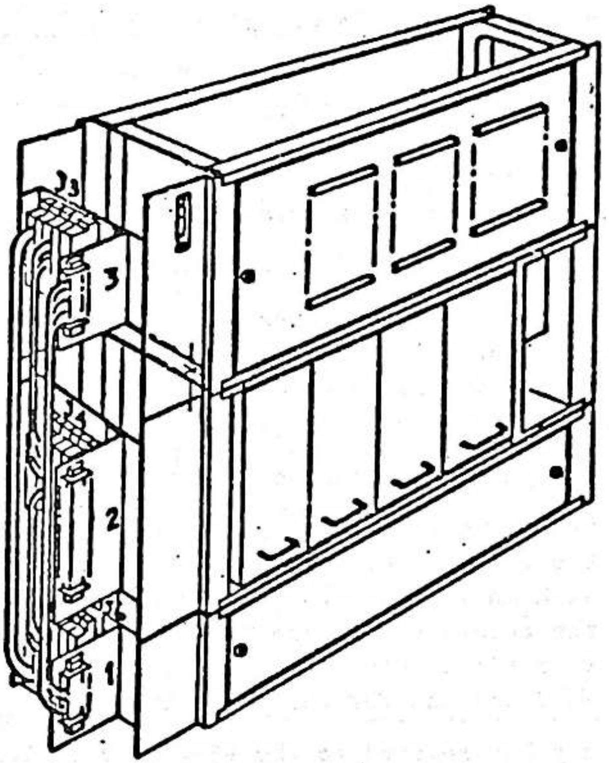

Fig. 1 - 1 Modules arrangement

1 Commands module
2 Adjustment module
3 Transformers module

The commnads module contains:

- the input a.c. protection fuses
- the input a.c. filters
- general line switch
- the command and signal circuits
- the service rectifiers for the +3V -3V voltages.

The transformes module contains:

- the supply transformes
- the d.c. voltages power rectifiers
- the auxiliary voltages rectifiers
- the breaker circuits for the slow voltage protection.

The adjustment module contains:

- the protection fuses of the d.c. voltages
- the switches to make the various power supplies work with an internal load instead of an external one
- the relays to measure the currents issued
- four adjustment boxes (two for the +5V, one for the -36V and one for the ±3V voltages).

Every box related to the +5V, -36V voltages contains:

- the switching transistor
- the switching transistor command circuit
- the current protection circuit
- the circuit for the fast voltage protection
- the levelling LC filter of the output d.o. voltage

The box related to the ±3V voltages contains :

- the power transistors
- the command circuits of the power transistors
- the shunt to measure the current
- the command circuits of the controlled diodes.

2. FUNCTIONAL DESCRIPTION

2.1. Performance principle of a switching power supply

The performance of the switching stabilized power supply may be understood considering the general diagram given in fig. 2-1.

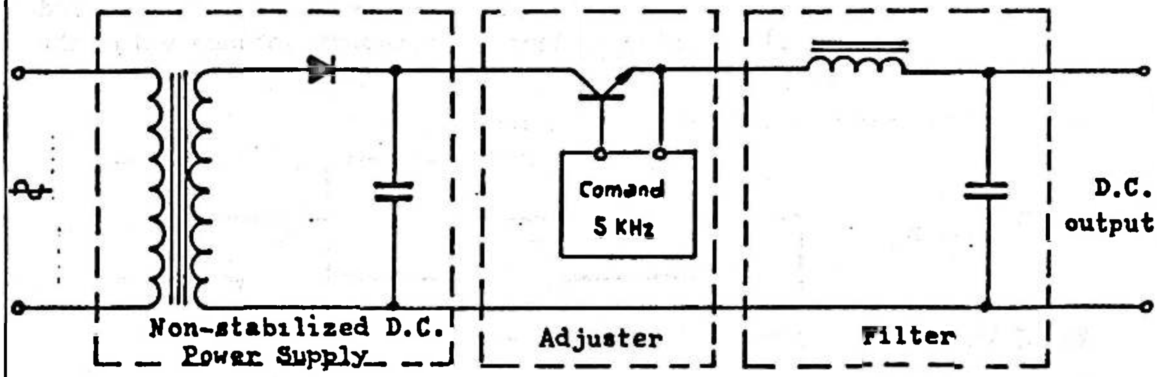

Fig. 2-1 - General diagram of a "switching" power supply.

It is divided in three main parts:

- the first consisting of a non stabilized d.c. power supply, supplies to the other parts a higher value voltage than the one required by the stabilized output;
- the second, consisting of a transistor which is used as a switch, supplies to the filter circuit voltage and current pulses at the constant frequency of about 500 Hz;
- the third, consisting of a filter circuit, integrates the voltage pulses received and supplies them in output under the form of a d.c. voltage whose value depends on the form of the pulses received.

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The transistor works at a fixed frequency of about 5000 Hz and, in nominal conditions of input voltage and with a certain output voltage, it loads the filter capacity and the user circuit, being on for about half a period and staying off for the remaining half period.
The filter capacity is loaded while the transistor is on and unloads on the users circuits when it is off.
If the output voltage has the tendency to decrease or to increase (because of a variation of the input voltage or the load current), a special circuit provides to increase or to decrease the transistor time-on within every period (fig. 2-2) in order to bring the output voltage value the nearest possible to the nominal value.

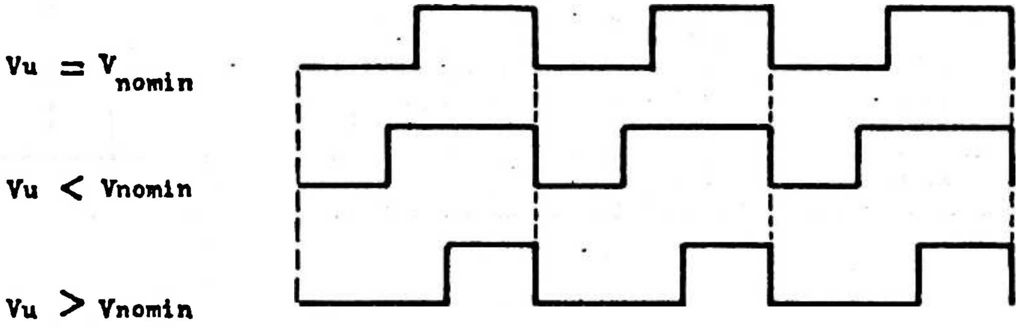


Fig. 2-2 - Command pulses for the switching transistor.

The filter capacity is loaded through inductance, in order to make the most constant possible the load current during the transistor time-on.
In this way, the capacity load voltage (and therefore the output voltage) is made proportional to the loading current application time.
Without the inductance, the loading current would reach a very high value at the beginning of the transistor time-on, so that the output voltage would immediately reach the value of the voltage supplied by the non-stabilized power supply.

2.2. Performance theory

The d.c. stabilized -36V, and the two +5.2V voltages are obtained bu means of a switching circuit.
The electric diagrams of the three circuits are substantially equal one another: they differ only in the values of some components which vary depending on the value of the voltage and the current supplied by every circuit.
Given the characteristics of the user load, each one of these circuits has the following characteristics:

- stabilization of the output voltage
- limits of the maximum current issued
- fast overvoltage protection
- protection from the lack of one or more phases of the power supply voltage.

2.2.1. Stabilization of the output voltage

In order to obtain a stabilized d.c. voltage, the related circuit performs the following operations:

- It compares a part of the output voltage with a constant voltage: the result of this comparison consists of a voltage, called "error voltage", which varies in function of the output voltage value;
- it compares the error voltage with a saw-tooth signal which ranges within the limits attainable by the error voltage.

The saw-tooth signal is generated at the constant frequency of about 5000 Hz.

The result of this comparison is a square-wave voltage which is at the low level when saw-tooth voltage is lower than the error voltage and it goes up to the high level when the saw-tooth voltage is higher than the error voltage. Fig. 2-3

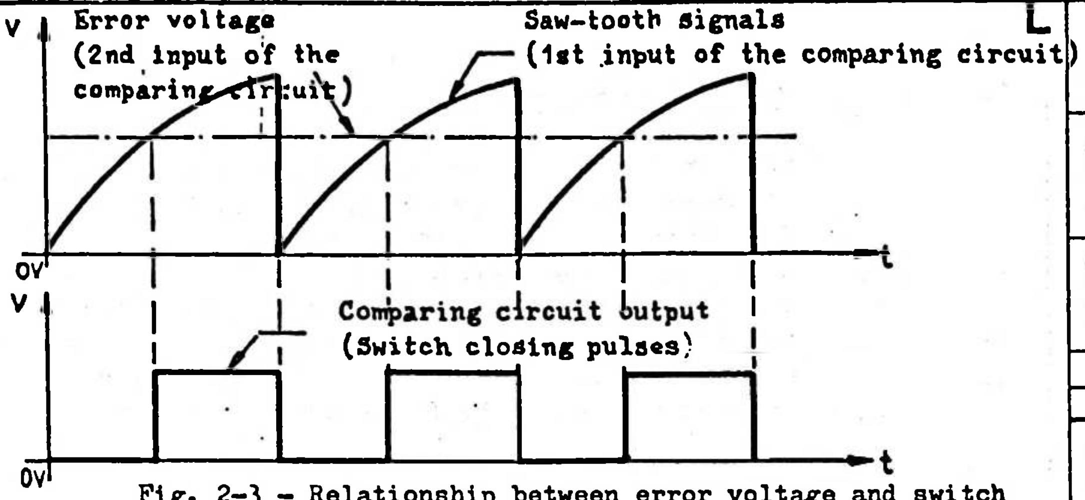


Fig. 2-3 - Relationship between error voltage and switch closing time.

It applies the square-wave signal to the circuit which performs the switch closing command.

The output voltage stabilization is obtained as indicated here below.
If the output voltage has the tendency to decrease, the error voltage decreases in turn and, as consequence, the switch closing voltage increases in order to bring the output voltage back near its nominal value, Fig. 2 - 4.

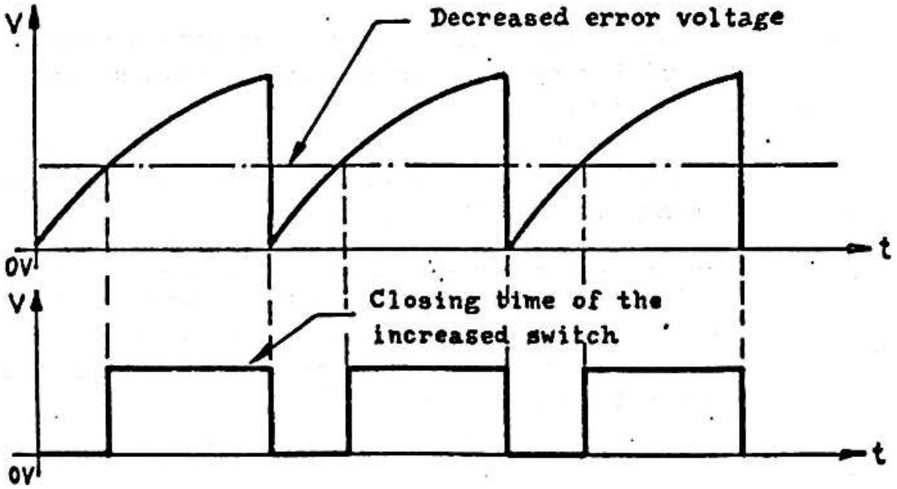


Fig. 2-4 Increase of the switch closing time in function of the decrease of the output voltage.

If the output voltage has the tendency to increase, the error voltage increases in turn and, as a consequence, the switch closing time decreases in order to bring the output voltage back near its nominal value - Fig. 2-5.

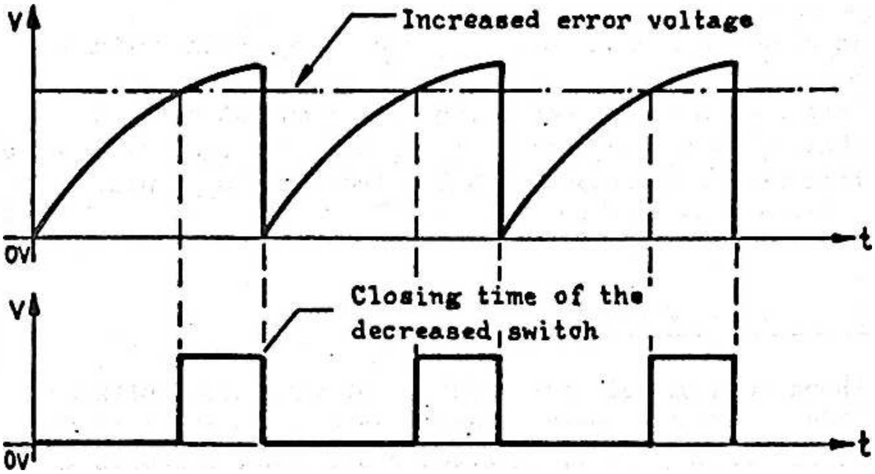


Fig. 2-5 Decrease of the switch closing time in function of the output voltage.

2.2.2. Current protection

The need for an adequate current protection derives from the fact that possible short-circuits and overloads may damage both the user and the power supply.
The circuit, performing the current protection, has been studied so that, once the current adjustment limit value has been reached, a further reduction of the load impedence corresponds to a decrease both in the voltage and in the current up to the extreme limit of the short-circuit at the ALI terminals, to which a zero volt output voltage and a current reduced to a few percentages of the nominal value correspond.
The mentioned circuit is sensitive to the current issued through a low value resistance set in series with the output. The voltage decrease at the ends of the resistance is therefore proportional to the current itself.
Once the adjustment limit is passed, this voltage (suitably amplified) acts on the switch transistor modifying its driving as described above.

2.2.3. Fast voltage protection

The users characteristics for the -36V, +5.2V voltages are such that in no case the maximum established voltage limits may be passed.
In order to guarantee what given above, each voltage has been supplied with a fast voltage protection.
This protection is sensitive to the output voltage so that, once the adjustment limit has been reached, the voltage itself is suddenly short-circuited to ground.
Intervention time 20 - 30 μs.

2.2.4. Phase lack protection

There is a circuit for each one of the three voltages: -36V, + 5,2 V which, should one or more phase of the supply voltage fail, intervenes and short circuits the output of its voltage using the same circuit of the fast protection.

2.3. Performance theory of a parallel adjustment power supply

The parallel type adjustment is obtained keeping constant the Vdc of the transistor parallel to the output, using the presence of an uncoupling resistance between the raw voltage and the output.
This is obtained comparing the output voltage (+3V) with a fixed reference voltage.
The error voltage drives a differential amplifier which controls, through an emitter-follower chain the parallel transistor.

2.4. Performance theory of a parallel adjustment power supply with SCR pre-adjustment

In addition to the parallel adjuster described above, the SCR pre-adjustment allows (for any value of the current issued by the ALI) to maintain constant, in static regime, the current in the parallel transistor.

2.5. Block diagram

The ALI 130/B power supply unit consists of the following main parts : DRW. 78C104361

- +5.2V voltage power supply (15,5A)
- +5,2V voltage power supply (12A)
- -36V voltage power supply (2A)
- +3 V voltage power supply (3.2A)
- -3V voltage power supply (8.2A)
- Command and block circuits

2.6. Switching power supply description

2.6.1. Voltage stabilizer circuit

2.6.1.1. Error detector and amplifier

The comparing circuit compares the output voltage with a reference voltage (D67).
It must be noted that the service voltages have their OV connected with the positive polarity of the output voltage. Fig. 2-6.

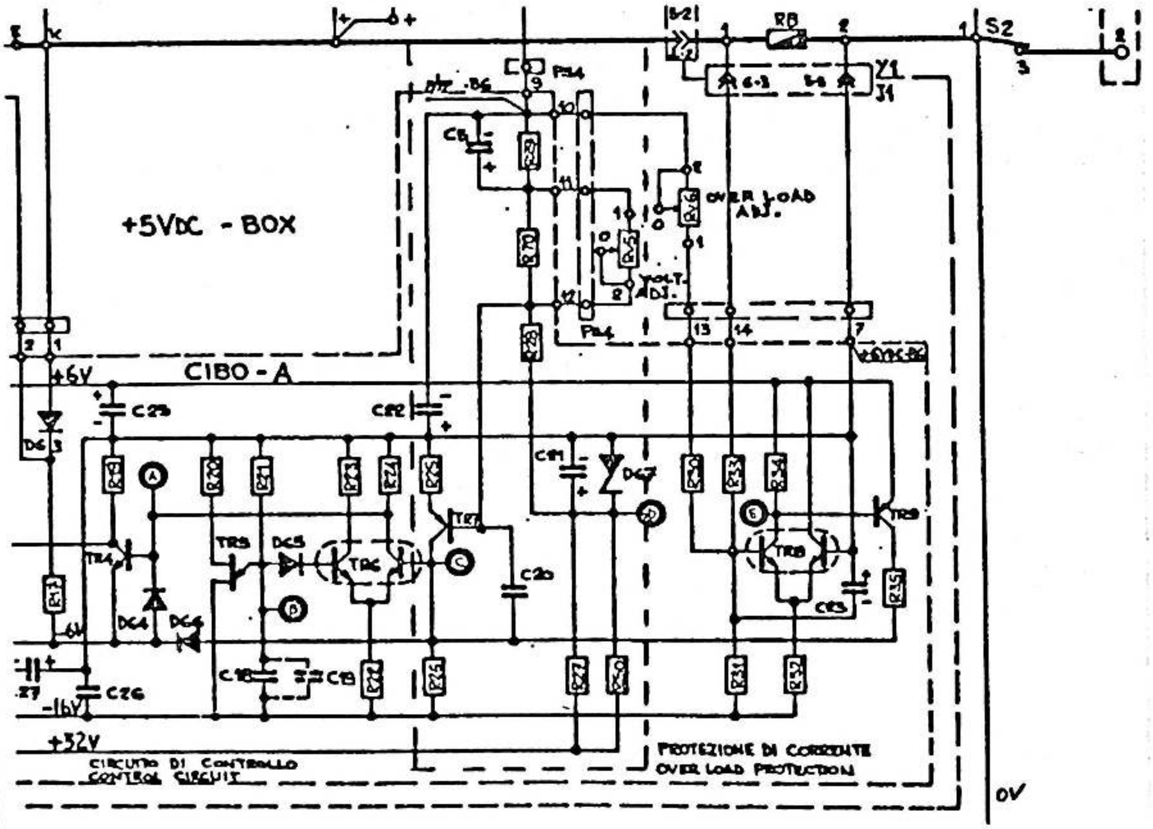


Fig. 2-6 Diagram of the comparing circuit for the output voltage.

With nominal output voltage, the TR7 transistor receives a slight negative polarization on the base.
The base current, amplified, circulates on the load resistor R26, determining an error voltage on the TR7 collector.

If the output voltage has the tendency to increase or to decrease, the voltage of the TR7 emitter increases or decreases of the same value.

As a consequence: if the output voltage tends to increase, TR7 assumes a more negative base potential and therefore the value of the error voltage increases.
If the output voltage tends to decrease, the contrary occurs. The D66 diode limits between -6V and -16V the error voltage.
The C20 capacitor is a counter-reaction in a.c. voltage.
The C21 capacitor is a filter for the +5.6V voltage obtained from the Zener diode D67.
The potentiometer RV5 allows the manual adjustment of the output voltage.

2.6.1.2. Saw-tooth signal generator

It is obtained with an oscillator which uses an unijunction transistor - Fig. 2-7

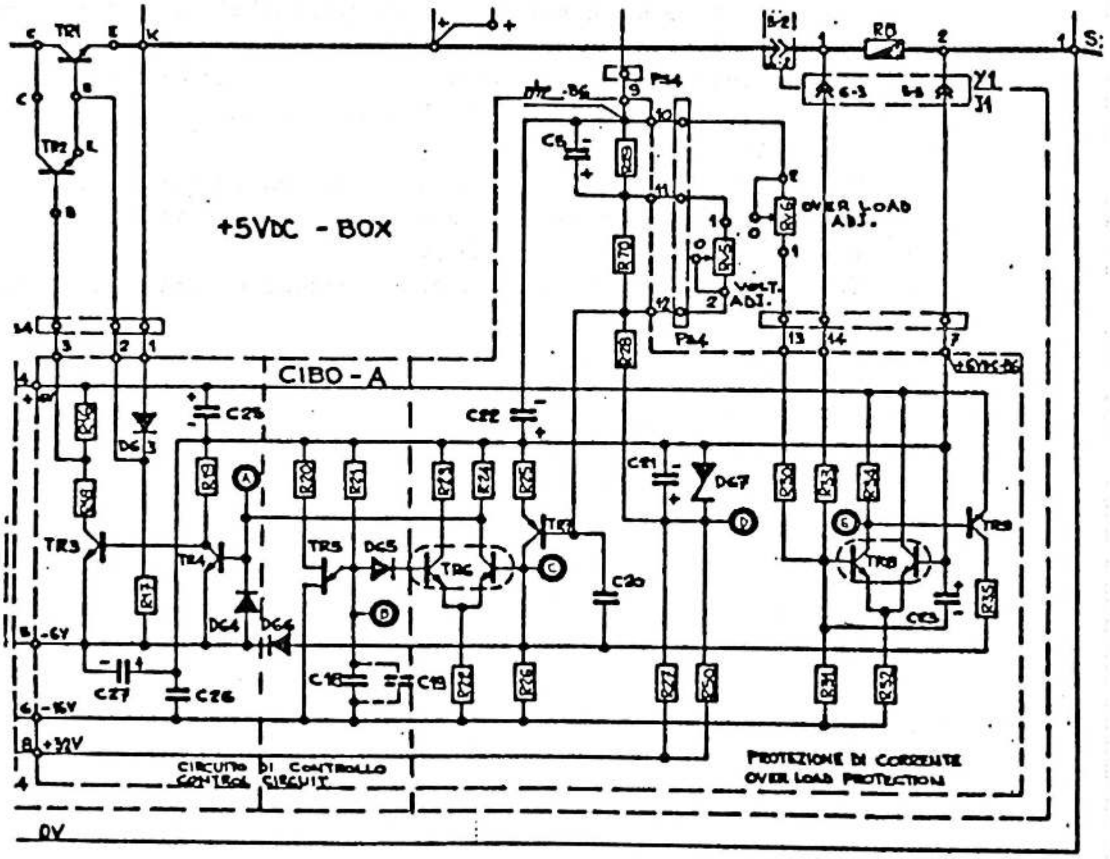


Fig. 2-7 Oscillator circuit diagram.

The C18 capacitor is loaded by the R21 resistor originating the leading edge of the saw-tooth; when the load voltage of C18 reaches the threshold of TR5, this last one turns on and unloads rapidly to -16V the capacitor originating the trailing edge of the saw-tooth.

Then TR5 goes back to its status, and the cycle begins again.
Fig. 2-8 gives the trend of the saw-tooth signal.

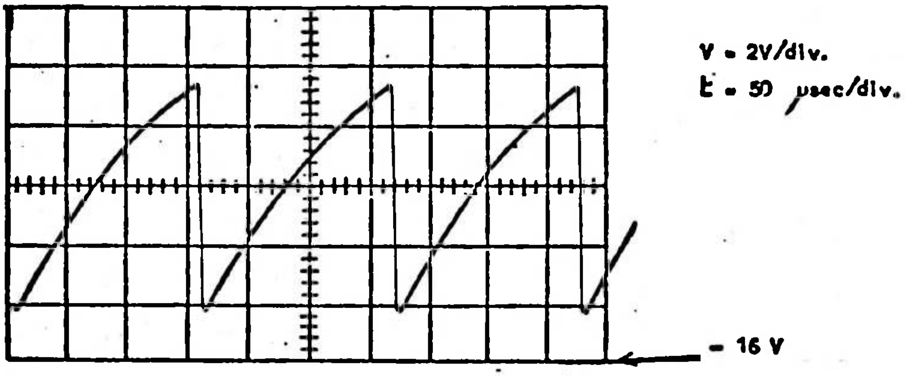


Fig. 2-8 Saw-tooth signal present on the TR5 emitter.

The frequency of this signal ranges between 4 and 7 KHz and may be varied modifying the time constant of the R21-C18 circuit. For this purpose, it is planned that a capacitor may be added in parallel to C18 when the oscillator frequency is above 7 KHz.

2.6.1.3. Comparison between error voltage and saw-tooth signal

The comparing circuit which performs the comparison between the instant value of the error voltage and the instant value of the saw-tooth voltage, is made with a differential circuit.
Fig. 2-9

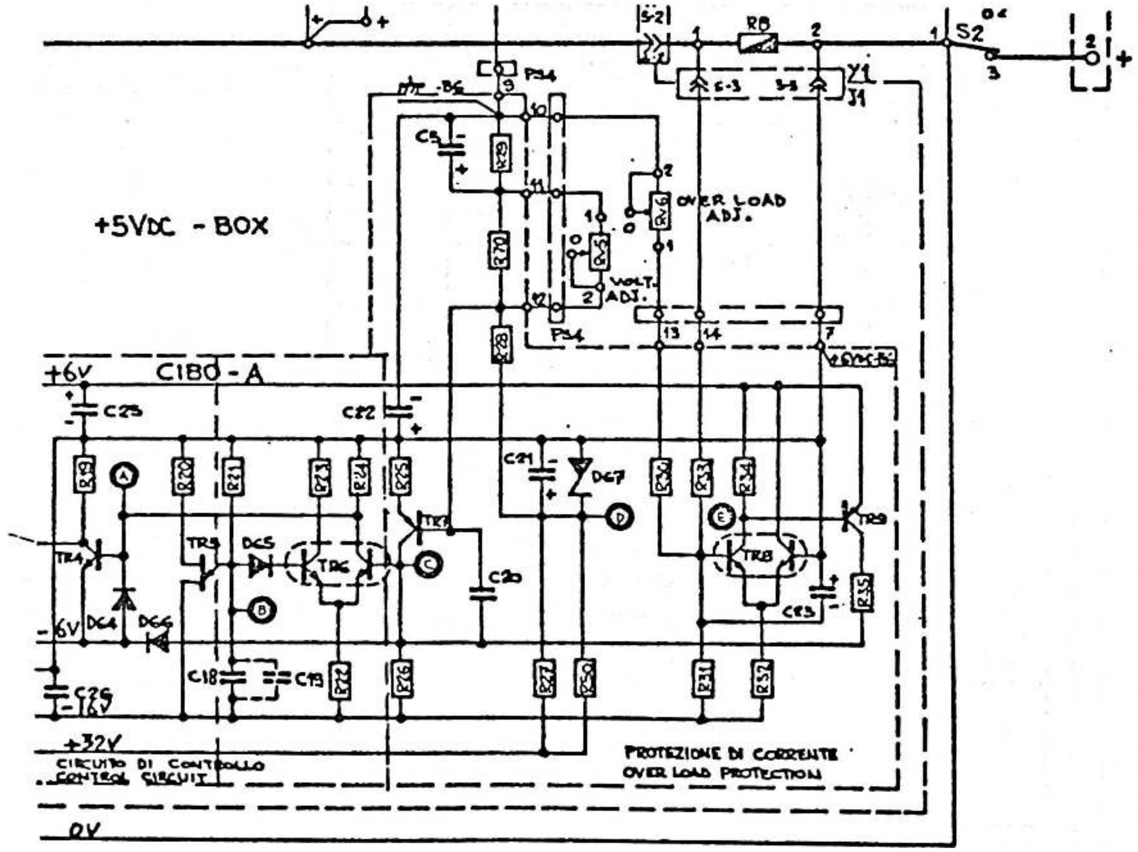


Fig. 2-9 Circuit comparing the saw-tooth and the error voltage.

The circuit is made in such a way to turn on the two transistors forming TR6 one at a time only.
When the instant value of the saw-tooth signal is lower than the instant value of the error voltage, the right section turns on and the output is low.

To the contrary, when the instant value of the saw-tooth signal is higher than the error voltage value the left section turns on and the output is high.

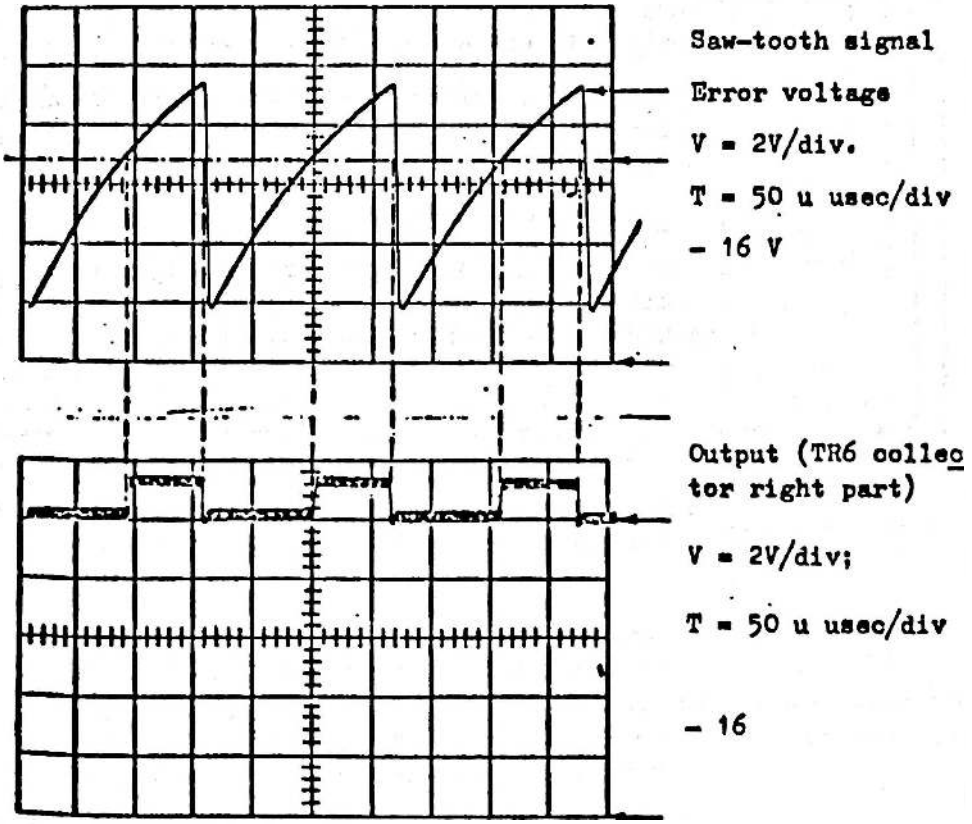


Fig. 2-10 Input signal and corresponding output of the comparing circuit saw-tooth-voltage error.

The output of the comparing circuit is used, after having been conveniently amplified, to drive the switching transistor.

- When the output of the comparing circuit is high, the transistor is on.
- When the output of the comparing circuit is low, the transistor is off.

Examining the fig. 2-10 the following can be seen:

- if the error voltage increases(when the output voltage increases) the time in which, for every cycle, the comparing circuit output stays high, decreases;
- if the error voltage decreases (when the output voltage decreases) the time in which, for every cycle, the comparing circuit output stays high, increases.

Therefore, the switching transistor closing time varies in order to maintain constant the output voltage.
The diode D65 fig. 2-9 is assembled as a protection to the TR6 left part base.

2.6.1.4. Command signal amplifier

The amplifier circuit consists of a double inverter.
Fig. 2-11.

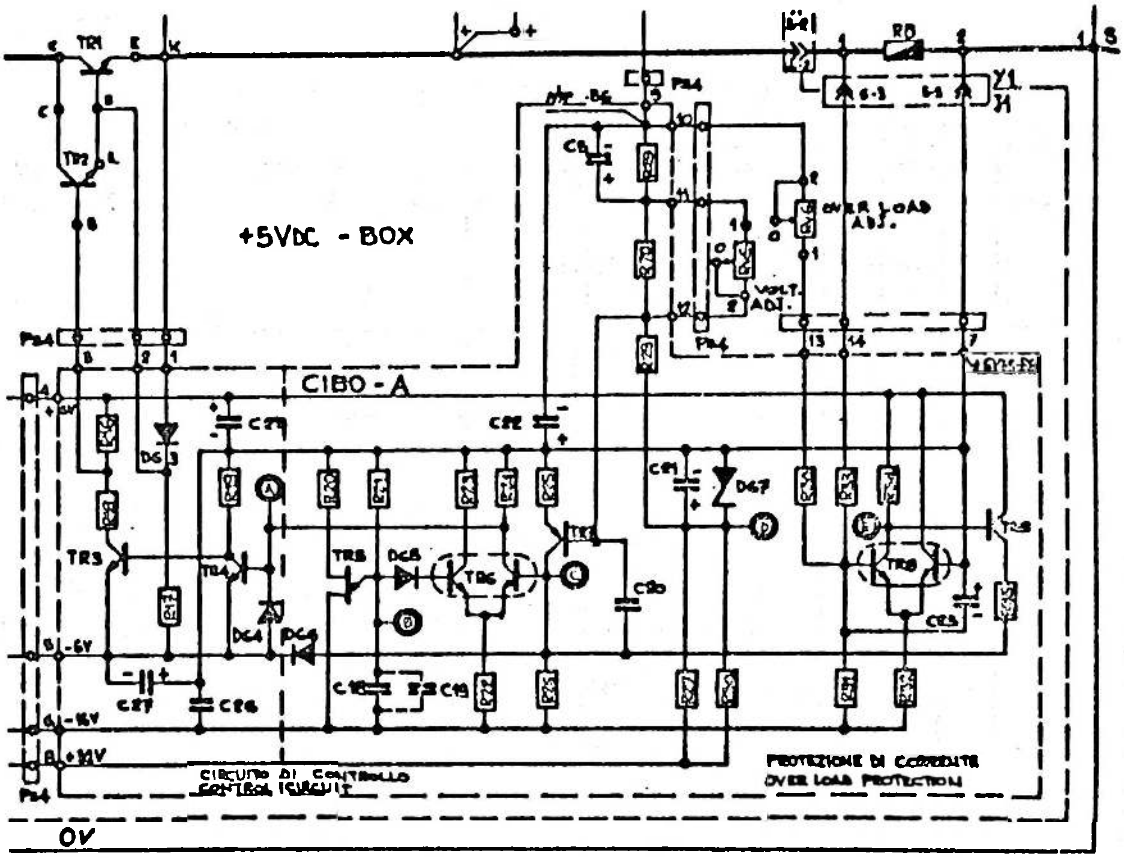


Fig. 2-11 Amplifier circuit for the switching transistor command signal.

The D64 diode limits to -6V the maximum negative excursion of the signal connected to the TR4 base.
Fig. 2-12 gives the input signals, the intermediate signals and the output signals of the amplifier circuit of the command signal for the switching transistor.

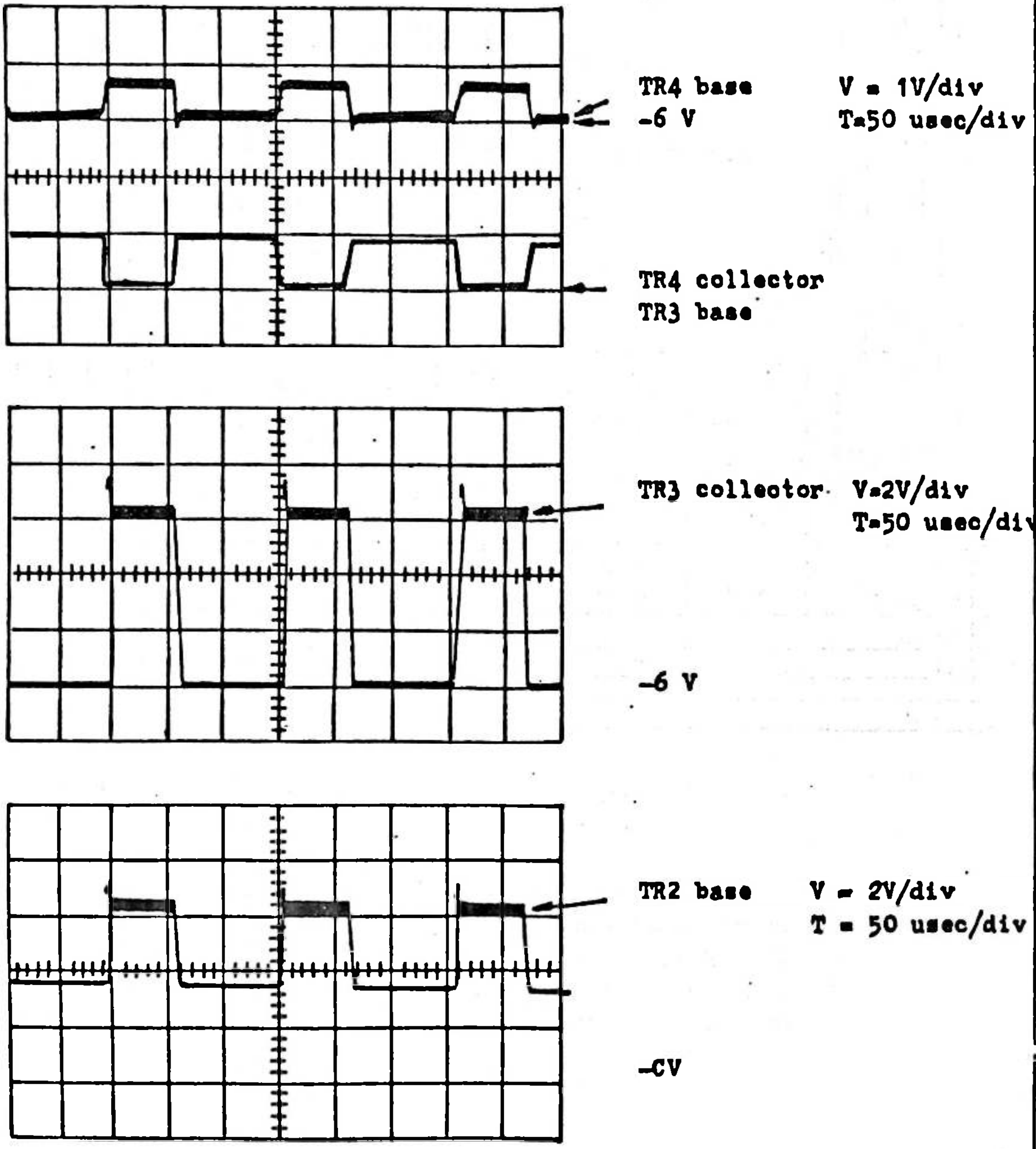


Fig. 2-12 - Signals on the TR3, TR4 transistors

2.6.1.5. Switching transistor

The TR1 transistor is closed when the command signal is high and is open when the command signal is low. Fig 2.13

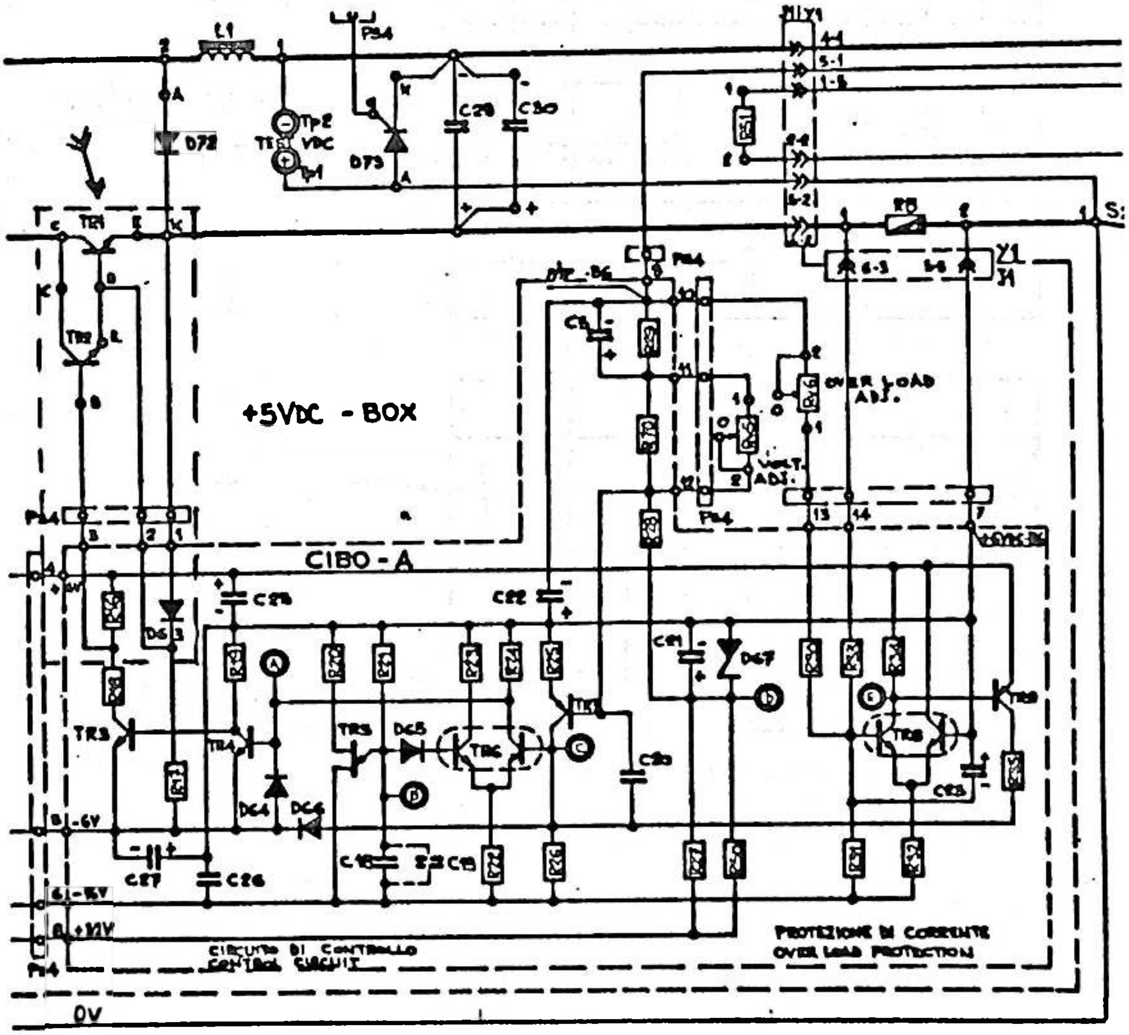
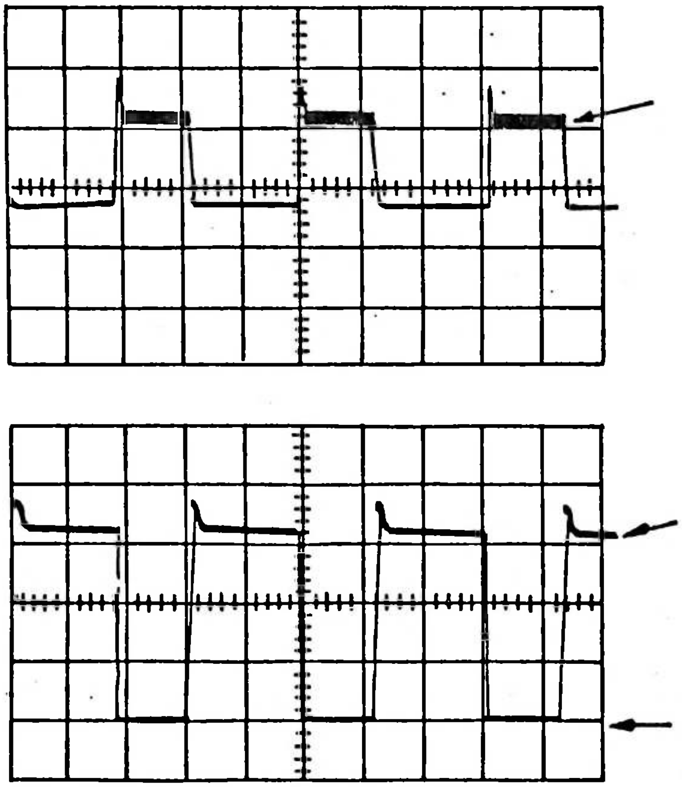


Fig. 2.13 Connection of the switching transistor with the other command circuits.

The D63 diode together with the R17 supplies a reverse polarity to the TR1 base when the command signal is low. Fig. 2.14 gives the command signal and the signal related with the opening and closing of the switching transistor.



Base and emitter of TR2

V = 2V/div

T = 50 usec/div

– 6V

TR1 collector

V = 5V/div

T = 50 usec/div

+ 5V output

Fig. 2-14 Signals in input and output of the switching circuits.

2.6.1.6. Power circuit

The power circuit consists of a secondary winding of a three-phase transformer, star-connected, which through a rectifying bridge loads the C2 capacitor with a d.c. voltage. *

Refer to fig. 2.15

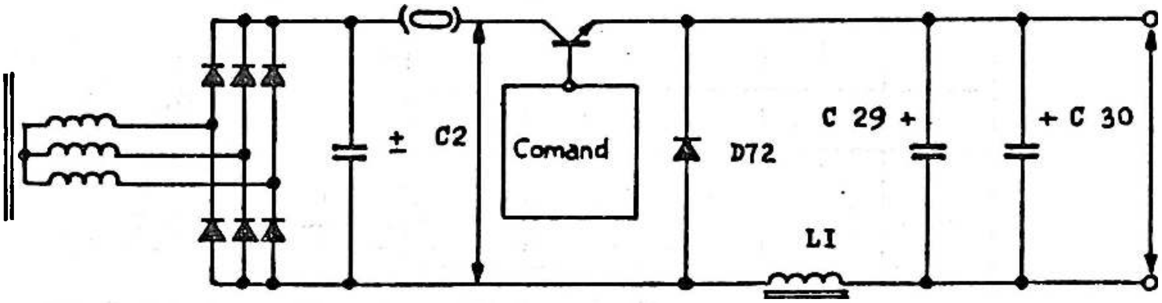


Fig. 2-15 simplified diagram of the power circuit.

This voltage is applied, through pulses, to the filter circuit L1 C29-30, by means of the switching transistor. When the switch closes, the capacitor is loaded through inductance.
When the switch opens, the energy stored in the inductance is unloaded on the capacitors through the diode D72.

* The diagram to which reference is made in the description is the one of the +5V voltage.

The output voltage ripple is given in fig. 2-16

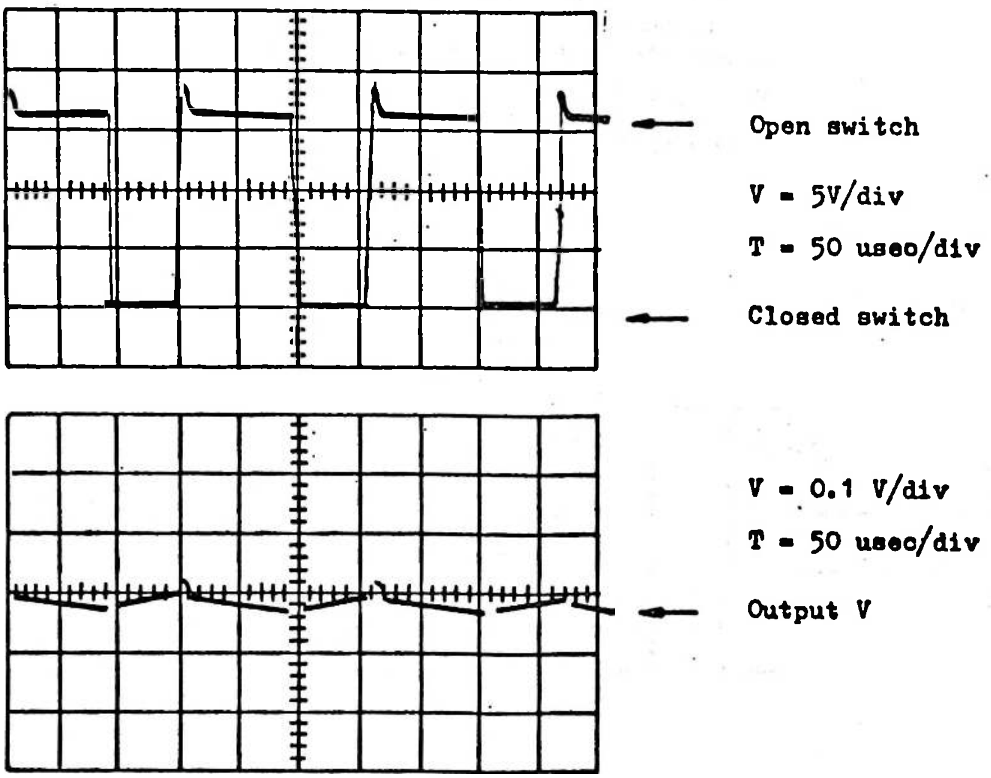


Fig. 2-16 Ripple in function of the opening and closing of the switching transistor.

2.6.2. Current limiting circuit

Fig. 2-17 gives a simplified diagram of the circuit performing the output current limit.

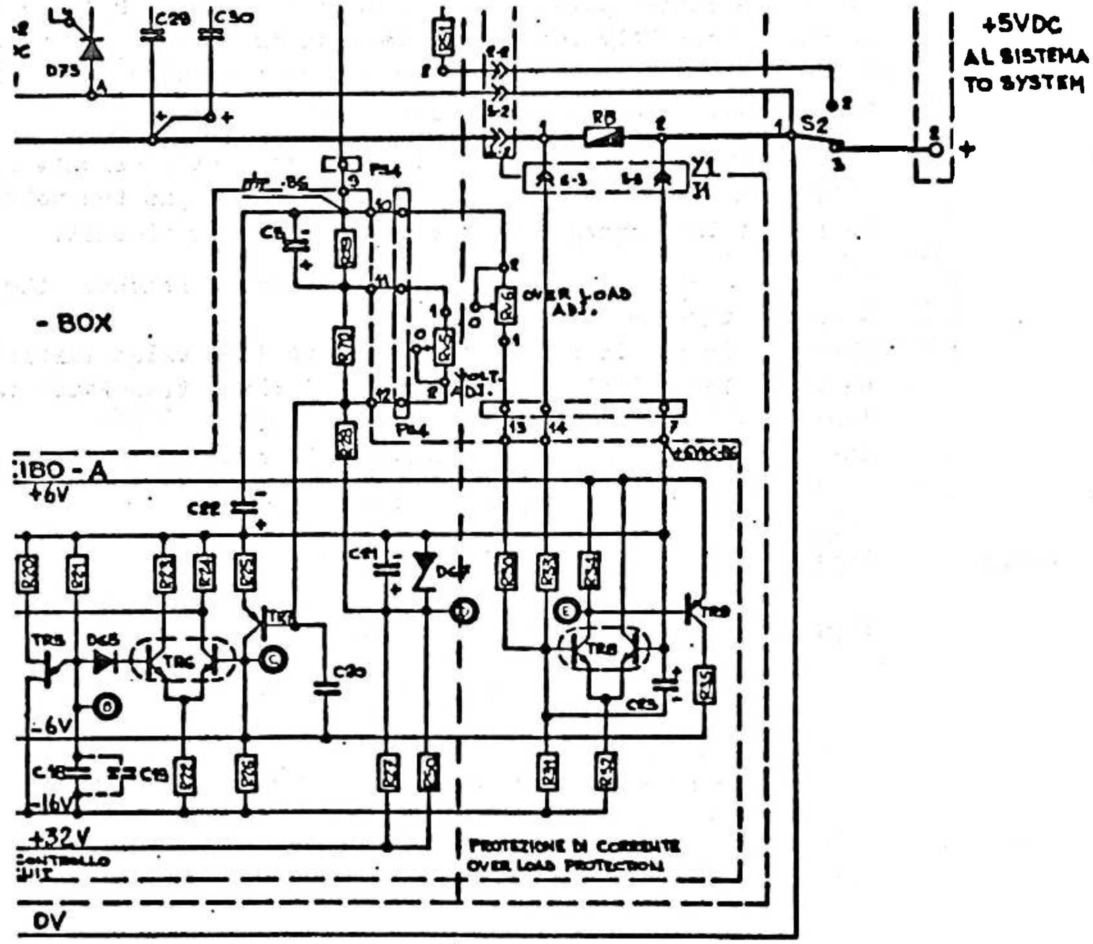


Fig. 2-17 Diagram of the output current limiting circuit.

The current issued by the power supply passes through the RB resistor (deriver from 60 mV) and its voltage fall is applied to the TR8 differential amplifier inputs.

In normal performance condition (issued current below the maximum) the left transistor of TR8 must be blocked and the right transistor must be on.
This is obtained polarizing the left transistor base to a potential slightly more negative than the one to the right through the RV6 potentiometer which acts through the resistive network formed by R30-31-33.

The TR9 output is applied to the TR6 comparing circuit input: with TR9 blocked, the circuit to stabilize the voltage is not influenced by the current limiting circuit.

When the current issued by the power supply reaches the adjustment value, TR9 is turned on.
When TR9 is on, it raises the error voltage value turning on for a lower period of time the switching transistor and lowering the value of the output voltage.
The adjustment is done by means of the potentiometer RV6.

2.6.3. Fast voltage protection

Fig. 2-18 gives the diagram of this protection.

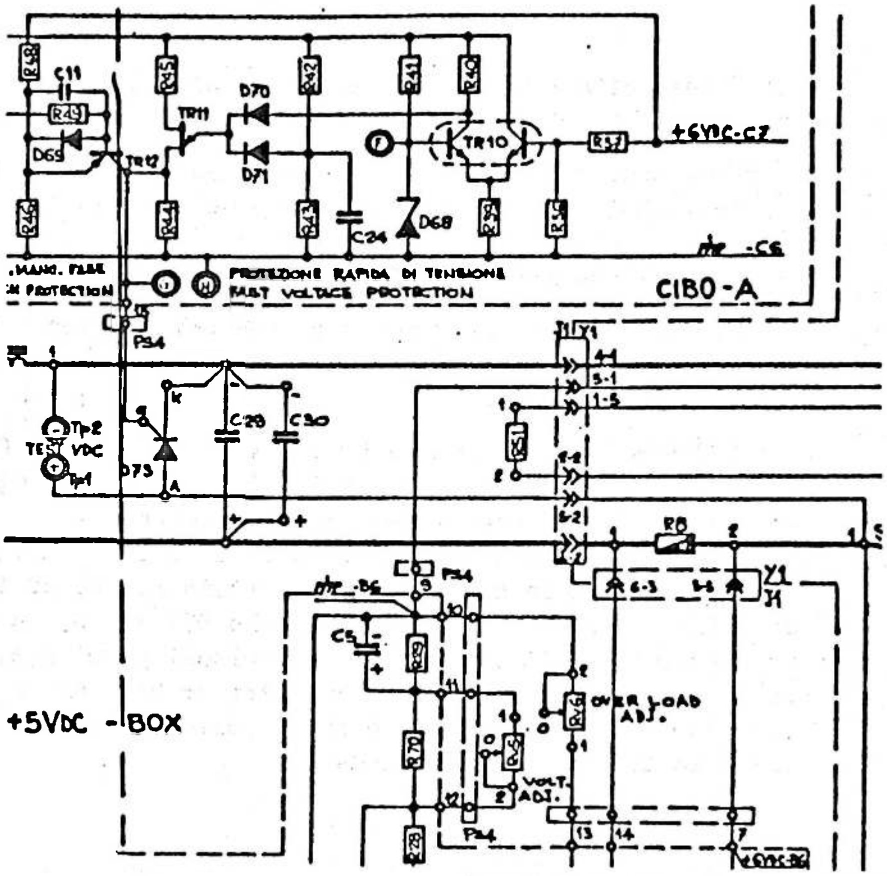


Fig. 2-18 Fast voltage protection circuit.

The circuit consists of:

- a comparing device (formed by TR10) which compares a part of the output voltage with a reference voltage;
- a threshold discriminating circuit (consisting of the unijunction transistor TR11) which acts when the voltage at its input reaches a certain value;
- a switch (formed by D73) which short-circuits the output of the power supply when it is issued.

The comparing circuit receives in input the constant voltage of the value of 5.6 ± 2V% (obtained with the D68 Zener diode and the R41 resistance) and in the other input a voltage, which is the partition between the output voltage, and the ⏚, obtained by means of a breaker (formed by R36 and R37); until the partition voltage does not pass the Zener voltage the left transistor of TR10 is off and the one to the right is on.

In these conditions, the collector voltage of the TR10 transistor is below the switching voltage of the unijunction transistor which stays blocked. When the partition voltage is above the Zener voltage:

1. the differential TR10 turns on the unijunction transistor TR11 which on its turn determines the switching on of the SCR D73.

The C24 capacitor is loaded by the voltage breaker formed by R42-43 to a voltage value below the one switching TR11 so that in normal conditions it has no effects.
In case of over voltage TR11 is turned on through the D70 diode, then, it is kept on for a certain period of time with the unloading of C24 through the D71 diode, as the holding voltage is lower than the switching voltage.
It is necessary to unload a capacitor to have an emitter current of TR11 with a value and a period of time sufficient to turn on the SCR diode.

2.6.4. Phase lack protection

The circuit that realizes this protection employs partially the circuit related to the fast voltage protection (Fig. 2-19).
The not levelled output of the bridge D59-60-61, in presence of all the three network phases, has a minimum level of 10V.
The absence of a phase is detected by the lack of the related semi-wave, during the period of which a zero voltage level corresponds (Fig. 2-20; 2-21).

In normal conditions (presence of the three phases) the transistor TR12 (whose emitter has a potential of about 4.5V) is off.

The phase lack turns on TR12 which acts on the fast protection circuit switching on the SCR.

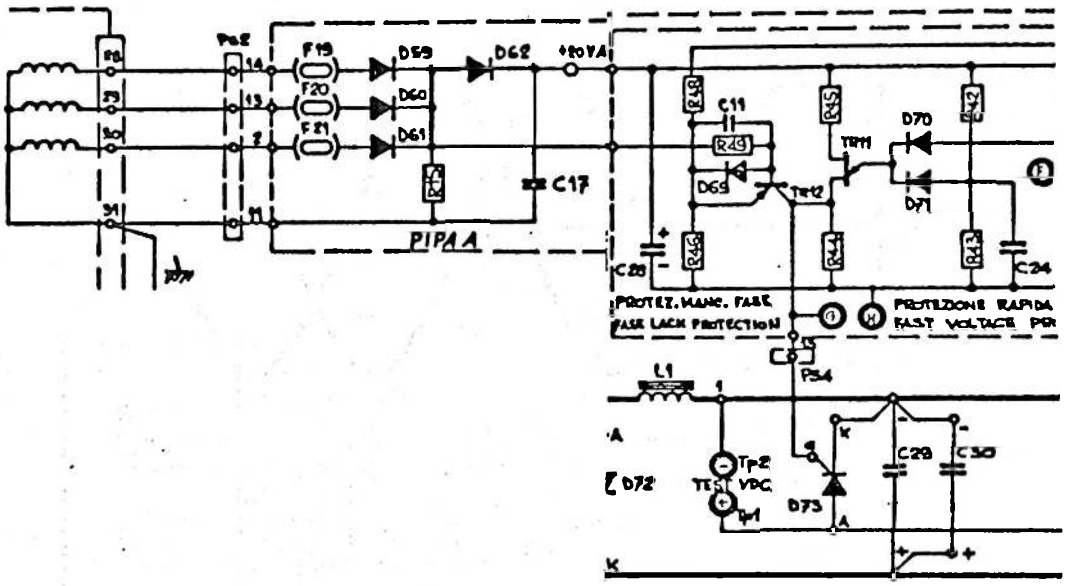


Fig. 2-19 Phase lack protection circuit diagram.

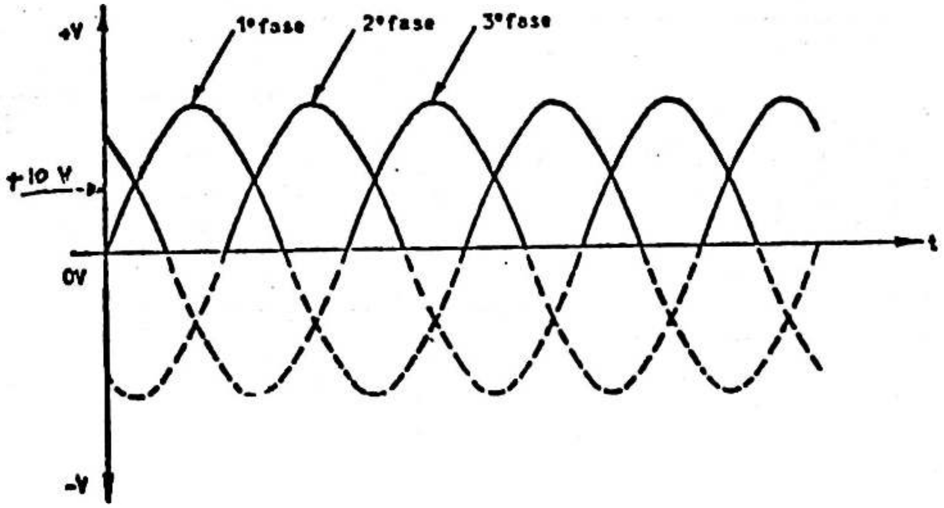


Fig. 2-20 Trend of the +20A signal when there are all the power supply phases.

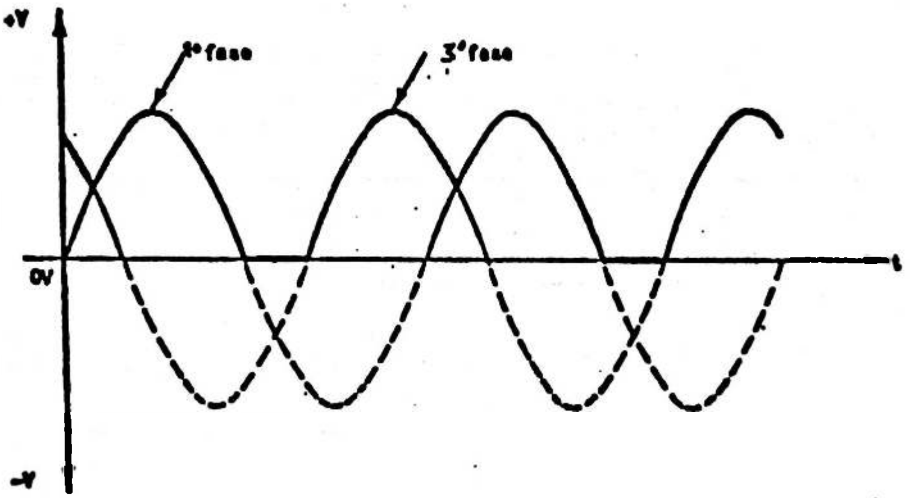


Fig. 2-21: Trend of the +20A signal when there is not one power supply phase.

2.6.5. Service power supplies

Every output voltage adjustment circuit receives the power supply voltages from four rectifier circuits which supply respectively +6V, -6V, +32V, -16V.
Fig. 2-22.

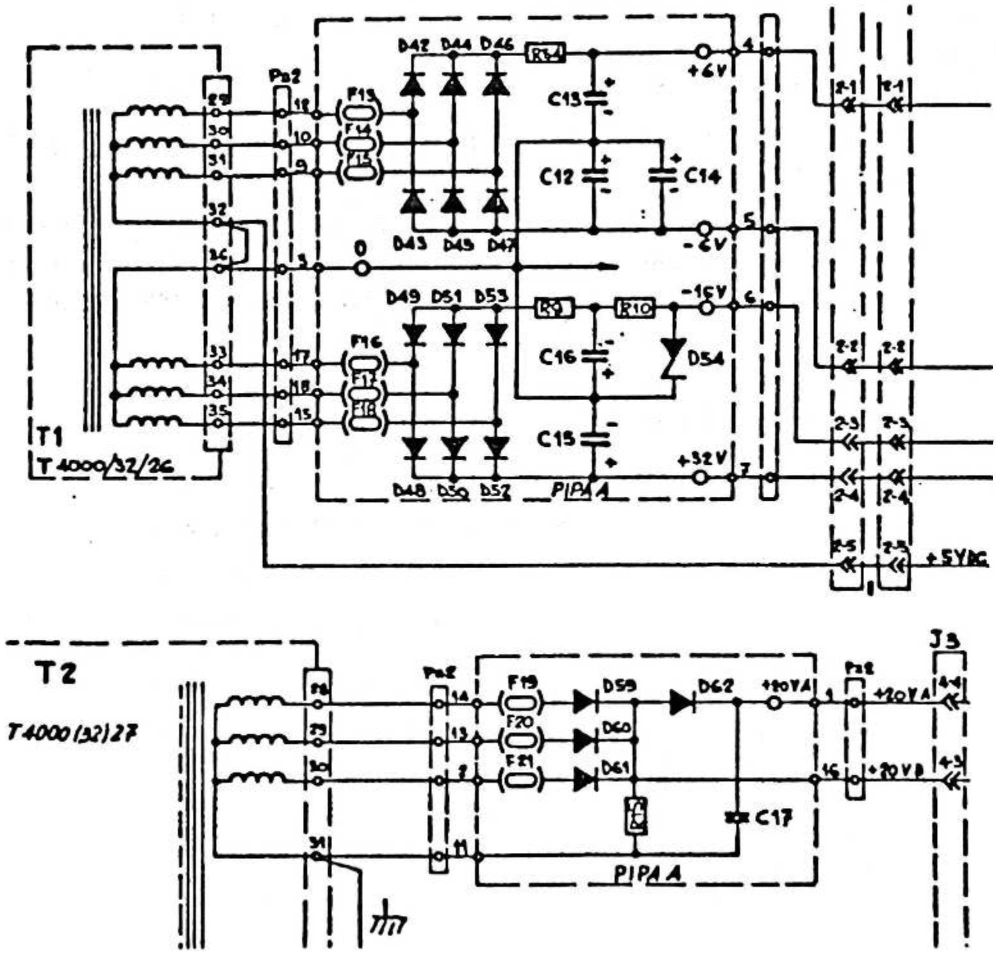


Fig. 2.22 Diagram of the service power supplies (the values of the voltages are equal for all the three output voltages).

These service power supplies have their zero volt connected to the positive pin of the output voltage.
The fast voltage protection circuit is supplied with a +20V voltage (called +20B) obtained from the +20A (used for phase lack protection) through an uncoupling diode which loads from filter capacitor so that the +20V voltage could go to 0V if one phase is lacking, without feeling the capacitor effect if it is loaded with +20V.
The zero-volt of the voltages +20A and +20B is connected with the negative pin of the output voltage.

2.7. +3V voltage - General

This voltage is obtained by means of a parallel adjustment system.

The power supply consists of four parts, the power rectifier, the parallel adjustment circuit and the stabilizer circuit and the auxiliary voltages rectifiers as indicated on drawing No. 78C104356 (page 2).

2.7.1. +3V power supply performance

The +3V power supply performance is described referring to the drawing No. 88C104356 page 2.
The output voltage (voltage at the terminals of TR23) is compared with a reference voltage (5.6V supplied by the Zener diode D82) through a breaker consisting of two resistors and a potentiometer R129-R130-RV15.
The differential amplifier TR21 and the chain of the transistors TR20-TR22 check the VCE of TR23, which corresponds to the output voltage.
A positive increase of the output voltage brings towards saturation the right section of the differential TR21.
The left section then tends to turn off, bringing on its turn towards saturation TR20 and with it the transistors TR22 and TR23.
The opposite effect is determined by a decrease of the output voltage.
The auxiliary rectifiers have the purpose to supply the error amplifier and give the reference voltage.

2.8. -3V voltage - General

This voltage is obtained by means of a nixed system of parallel adjustment and S.C.R. pre-adjustment (drawing No. 78C104356 fig. 1).
The power supply consists of :

- power rectifier
- stabilize circuit
- SCR command circuit
- current control circuit in the parallel adjuster
- rectifier of the auxiliary voltages.

The voltages pre-adjustment has been introduced to reduce to the minimum the dissipation in the parallel transistor in any load condition.

2.8.1. Performance of the -3V power supply

The stabilizing of the output voltage is obtained with the same system given in para. 2.7.1.
In this power supply the rectifier voltage, which goes to supply the adjustment transistor, is variable in function of the load current through the pre-adjustment SCR.
In this way, the adjustment transistor is always on because of a constant current, independently from the load network variations.
The command of the controlled diodes is obtained by means of a trapezoid shaped wave voltage (obtained from an auxiliary double semi-wave rectified voltage and a Zener diode (D83)).
This trapezoid shaped wave goes to supply the Unijunction transistor TR13 generating the driving signal for the controlled diodes.
Checking this signal, it is possible to reduce the voltage so to maintain constant the TR19 transistor current.
The current circulating in the TR19 transistor passes also through the R132 resistance.
The voltage is compared, through a breaker consisting of R112 RV13, with a constant positive voltage (6.8V D78).
Adjusting the potentiometer RV13, through the transistors chain TR15-TR14, the signal to drive the controlled diodes may be checked and the value of the current circulating in TR19 fixed.
A current variation on the load is felt by the parallel adjusting transistor TR19 which must react with consequent voltage variations at the terminals of R132. If the voltage at the terminals of R132 decreases (for example : because of an increase in the load current), TR15 and TR14 tend towards being turned off.
The C46 capacitor is loaded as a consequence in a period of time which is lower, anticipating the command signals to the SCR.
The increase which is thus obtained on the output voltage of the bridge is such to bring the current in TR19 back to the previous value.
In our case, the current circulating in TR19 must be adjusted to 2A detectable measuring between ⏚ and the test point from IC with a voltmeter (the voltage measured is of 0,2V).

If the volatge at the terminals of R132 tends to increase the circuit behaves inversely respect to what described above.
The auxiliary rectifiers have the same functions of those of para 2.7.1.

2.9. Control and commands circuits

2.9.1. Overtemperature protection

The ALI 130/B power supply has eight devices protected again overtemperature through thermostats. These devices are:

- transformers T1-T2, which have each one three thermoswitches, connected in series and set on the three primary windings; these thermostats open when the temperature is above the 110°C.
- The transformer T3.
- three switching transistors, which have a thermoswitch, each adjusted to 75°C.
- two parallel adjusting transistors with a thermoswitch each one adjusted at 75°C.
  On the dissipator of the power supply bridge of the -36 voltage there is a thermoswitch adjusted at 75°C.

The opening of any one of the thermoswitches causes the falling of the TL1 relay and the switching on of the signal lamp set on the commands module.
In case of overtemperature with the opening of a thermoswitch (fig. 2-23) the controlled diode D91 is on and on its turn it brings to ground the collector of TR26 making TL25 open with related de-energizing of RL2.
The de-energizing of RL2 causes the opening of RL1 (D90 is always closed during performance) and then the switching off of the power supply with subsequent switching on of the TEMPERATURE and ALERT lamps set on the commands moudle.

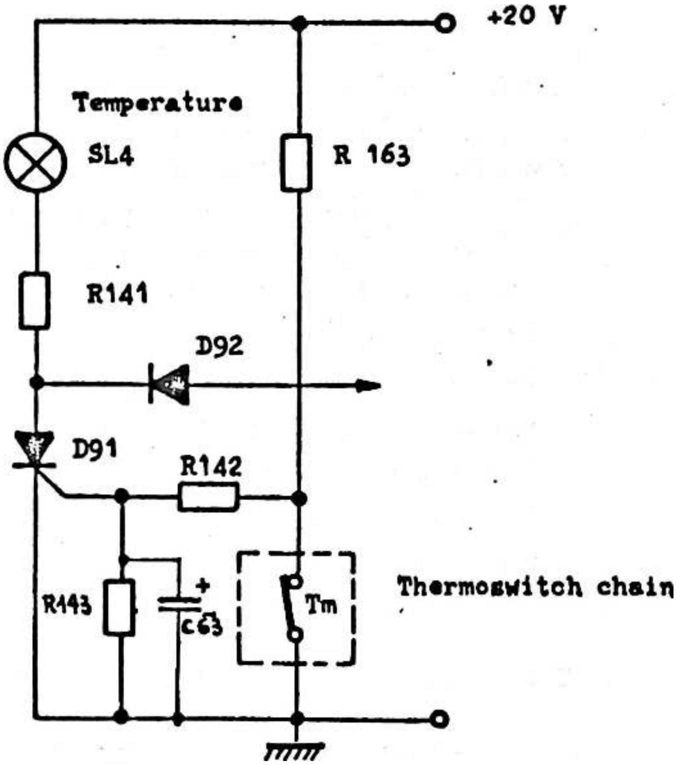


Fig. 2-23 - Overtemperature circuits

2.9.2. Slow voltage protection circuits

When one or more output voltages of the ALI 130/B exceed in positive sense or in negative sense, the limit of 8% of the nominal value, a special circuit intervenes which deenergizes the TL1 power supply relay.

This circuit is called "slow voltage protection" as from the moment in which the relay acts to the moment in which it is de-energized 50 msec elapse after a variation in voltage exceeding 8% has occured.
Every voltage to be protected is supplied with two similar circuits, the output of which is set in OR.
They intervene:
- one when the voltage exceeds the nominal value by 8%;
- the other when the voltage is 8% below the nominal value.

In order to check when the voltage exceeds one of the given limits, a voltage breaker and a comparison circuit are used.
The voltage breaker:
- at one terminal receives the voltage to protect
- at the other terminal it receives a reference voltage of the value of 10V and with a sign opposite to the one of the voltage to protect.
- from an intermediate point it supplies a voltage of about 0V.

This point varies in function of the value of the voltage to protect, according to the reduction ratio introduced by the resistances network.

The comparison circuit is realized with a differential amplifier which compares the voltage of about 0V supplied by the voltage breaker with one 0 V fixed.

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In order to perform the +8% protection (drawing N° 78104358) in nominal conditions, a voltage slightly negative with respect to the 0 V is taken from the breaker by means of the RV4 potentiometer and it is applied to the input 4 of the differential so that input 3 is positive with respect to the other and the output is low.
When the voltage reaches and exceeds the adjustment level, of +8% the amplifier output goes to n+5V sending a de-energizing command pulse to the holding circuits of the TL1 relay, set on the commands module.

In order to perform the -8% protection, in nominal conditions, a voltage slightly positive with respect to the 0 V is taken from the breaker by means of the RV3 potentiometer and it is applied to input 7 of the differential so that the input 6 is positive with respect to the other and the output is low.

For lower voltage variations (-8%)the circuit performance is perfectly similar.
The amplifier output used for the +8% protection is connected in OR with the output of the amplifier used for the -8% protection of the same voltage. The two amplifiers are set within the same container.
The differential amplifiers are supplied by two stabilized voltages, which have the value of +12V and -6V.
These voltages are obtained by means of Zener diodes respectively from the voltages +20V and -10V supplied.
The first from the +20 of the CPU, the second is taken by the Zener diode D115 I.II.
The circuit consisting of R68 and R69 makes the slow protection intervene in case the -10V voltage is lacking.
In fact, when both +12V and -6V voltages are present, the voltage breaker consisting of R68 and R69 sends to the anode of D39 a voltage of about 0 V, while if the -10V and therefore 6V is not present, the same breaker sends in output a positive voltage.
The diodes in parallel to the differential amplifiers inputs have the purpose to avoid that the potential difference between the inputs themselves assumes high values in case a power supply is disconnected. In this case, the breaker stays connected only to the reference voltage and it is this value which is applied to the used input.

The output of the signal which is sent to the commands module to drive the de-energizing circuits of TL1, may be short-circuited to ground, setting a strapping between the terminal pin 1-1 and the terminal pin 1-2 of connector J2.

This operation allows to exclude the slow voltage protection intervention, should it be necessary.

(Drawing No. 78C104357).

If the voltage goes out of service, the voltage protection set for its control, sends to the base of TR26 a positive signal.
This signal saturates the TR26 transistor which on its turn turns off TR25 with subsequent de-energizing of RL2.
The de-energizing of RL2 causes the opening of RL1 (D90 alwaysclosed during performance), the switching off of the power supply and the switching on of the ALERT lamp.

2.9.3. Power supply circuit of the a.c. voltages

On drawing No. 78C104357 there is the diagram of the circuit which checks the sending of the a.c. voltages to the transofrms T1-T2-T3.
To supply the above mentioned transformers it is necessary that the TL1 relay is energized, which is conditioned by the RL1 excitation.
With the switch S8-A in position ON, the RL1 relay is energized through the resistor R161, by a d.c. +20V voltage (supplied by CPU).
If the power supply works regularly also RL2 closes and the relay TL1 stays energized.

When switching on with a power supply out-of-service (the output voltages which are at their nominal value or opening of a thermo-switch) the relay RL2 will remain de-energized.
The relay RL1 will stay energized until the timer TR24 does not intervene which closes the SCR diode D90 with subsequent de-energizing of RL1, of the TL1 relay, and switching on of the ALERT lamp.
The time after which the timer intervenes, in case of malfunctions when switching on is of ≅ 2 sec.

2.9.4. Disconnection of a voltage from its external load

In order to have it work correctly every voltage of the ALI 130/B needs a minimum loa connected with the output, such to cause a minimum current of at least 1/10 of the maximum current which can yielded.
When one or more voltages of the power supply must work without external load (in case of adjustment or failure

search) it is alwys necessary to apply a minimum load to the voltage under exam.
To simply this operations there are five switches (S1-S2 S3-S4-S7) placed on the back of the adjustment module, which allow to supply a load:

- exeternal in position 1-3

- internal, in position 1-2 Fig. 2-24.

For the switches S4-S7 the connection of internal load is not planned, as the two voltages +3V -3V may work being empty.

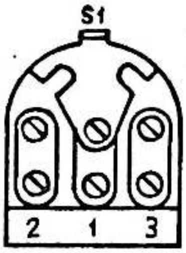

Fig. 2-24 - Breaker.

2.9.5. Signals towards the output

The power supply, besides supplying the stabilized d.c. voltages -36V, ±3V, +5.2V supplies or searches for some control signals and conditioning towards the controller of the DSC157 dis. N° 78C104357.

The signals are:

- EXTEU
- +20V EXT
- SGALA
- ALER
- CONS 1 AND CONS 2

2.9.5.1. EXTEU (HEARDS EXTENDED)

The signal EXTEU in the unit powering off phase makes the decrease the voltage (both A.C. and D.C.) supplied by the unit, depend on the previous unloading of the heads. This signal arrivies from the disc handlers and is at ov for loaded heads.

2.9.5.2. +20 EXT

Voltage which is supplied by the CPU to switch on the power supply.
The power supply, once it has been turned on may work also without the +20 EXT.

2.9.5.3. SCALA

0 V logic level voltage +5V.
With switched off power supply it is 0 V, with working power supply it is +5V.

2.9.5.4. ALER

Logic signal +10V or 0 V which is sent to the controller of the DSC 157.
This signal is supplied by Ie 50, which checks the voltage +20 EXT in the tolerance limits +8% (drawing No. 78C104357).
If the voltage +20V EXT is in the ±8% tolerance limits the signal is of, if the voltage is out of limit the signal is 0 V.

2.9.5.5. CONS 1 - CONS 2

They are supplied with the power supply working, they drive the ALI 260 DP causing the closing of the relay of the a.c. power supplies to the disk handlers.

Honeywell
Honeywell Information Systems Italia

DSS 157

DISC STORAGE SUBSYSTEM

Installation

Second Edition

A Field Engineering
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1. INTRODUCTION

The purpose of this manual is to furnish a sequence of operations to optimize the installation of the DSS 157 disc storage subsystem.
These operations presume that the site has been adequately prepared, according to the requirements quoted in the Site Preparation Manual, but do not directly consider the configuration of the system.
The installation team will draw all necessary information from the following two auxilirary documents, individual to each installation:

- Site layout

  Giving the collocation of the subsystems in the site and showing those accessories which, though not normally supplied with the subsystems, are necessary to overcome particular space or operative problems (i.e. extra low level cable ducts, cable ways and so on).

- Unified Subsystems Connections

  The forms bearing the above name give information upon the connection of the subsystems to:

  - the CPU, MPA (or 2nd MPA) or MPS connectors
  - the centralized DC power supply
  - the AC supply breakers
  - the fan supply and their control terminal board
  - the AC power supply control circuit.

The Unified Subsystems Connections (USC) forms also give details on the insertion of calibration plugs and terminators.
A detailed description on how to use the USC forms will be found in the CPU Installation Manual.

> **Note**
>
> For all materials necessary for the mechanical and electrical assembly, cross refer to the "Cables and Parts" Kit Lists.

The final subsystem check-out must only be done if the structural and electrical connections have been completed and if the check-out of the Central Processor and program loading subsystem has been accomplished.

2. TOOLS AND INSTRUMENTS

2.1. - INSTALLATION TOOLS AND INSTRUMENTS

The operations to be performed to install this disc storage subsystem may be carried out with the use of the following equipment:

- Engineer's tool kit
- Site tools
- Bushing type pliers P.N. 4355406 G (Area tool level)
- Scratch dispac.

2.2. - SPECIFIC DSU 167 TOOLS

The following list shows tools specific to the DSU 167 that will only be needed in case incompatibility or particular faults should arise. Such material need not necessarily be stocked at site level:

- C.E. Pac
- DSU Tester
- Alignment tool
- Cap carriage tool
- Syringe
- Jumper
- Test probe, Geaps
- Paddle
- S/driver end bit

2.3. - SPECIFIC DSU 157 D TOOLS

The following list shows tools specific to the DSU 157 D that will only be needed in case incompatibility or particular faults should arise. Such material need not necessarily be stocked at site level:

- C.E. Pac
- Head alignment tool
- R3YBA PWB (P/N 60200816-001) or 1:1 probe
- Block adjust zero track
- Block adjust fully retract
- Gauge Hd. position alignment
- AMP 465195 Z pin remover
- Bar position alignment
- Gauge position alignment.

2.4. - SPECIFIC DSC 157 TOOLS

- VAR 583
- Special Pewer Supply box boards jumper

3. ACCEPTANCE AND COLLOCATION

3.1. - PACKING

The subsystem is shipped to its destination in a number of crates equal to the number of drive units plus one for the DSC 157.
External to each packing crate, are affixed forms giving:

- the contents of the crate
- the guide to uncrate and remove the wooden battened transport base (" pallet" or "shipping skid").

3.2. - ACCEPTANCE

Upon receipt, all packages are to be visually examined for damage. If any damage is noticed, it will be necessary to:

- have the carrier witness the entity of the damage
- submit a detailed report to headquarters
- fill-in any enclosed shipping forms.

Note

The DSC or DSUs should not result under Surveillance Plan or other Analysis. However, should they be, ascertain that all documents pertinent to the analysis or plan are available.

3.3. - UNCRATING

- Ensure that the subsystem is uncrated as per rules set out by the uncrating guide, attached to the outside of the crate.
- Ensure that the contents tally with the description.
- Remove the documents and accessories, contained in the crate, and set them aside so as not to impede the installation operations.

- Set aside the following kits :

3.3.1. - DSC 157 to System Connection Cables

- DSC 157 (50 Hz) "Cable Kits" P.L. 78X103827 : Col. G1 (6 m), G2 (8 m)
  Col. G5 (2nd MPA), G7 (MPS)
- DSC 157 (60 Hz) "Cable Kits" P.L. 78X103827 : Col. G3 (6 m), G4 (8 m)
  Col. G6 (2nd MPA), G8 (MPS)

3.3.2. - DSU 167 (ADU 157) to DSC 157 Connection Cables

- DSU 167 (50 Hz) "Cable Kits" P.L. 78X103856 : Col. G1 (1st DSU 167)
  Col. G2 (2nd DSU 167)
  Col. G3 (3nd DSU 167)

Note

Ascertain that plugs No. 0-1-2 (1st DSU), 3-4-5 (2nd DSU) and 6-7-SP (3rd DSU) have been included.

3.3.3. - DSU 157 D to DSC 157 Connection Cables

- DSU 157 D (50/60 Hz) "Cable. Kits"
  P.L. X78106807 : Col. G1 to G9 (1st to 9th DSU 157 D)

Note

Ascertain that all the necessary plugs (No. 0-1-2 .....6-7-S) have been included.

3.3.4. - DSU 157 D Connection Cables in Case of DSU 157 D Add-Ons to DSS 157 with DSU 167 Drives

- Mixed DSUs (50/60 Hz) "Cable Kit "
  P.L. X78106810 : Col. G1 (DSU 157 D following the 1st DSU 167 Cluster)

  Col. G2 (DSU 157 D following the 2nd DSU 167 Cluster)

3.3.5. - DSS 157 Part Kits

- DSS 157 (50/60 Hz) "Part Kits"
  P.L. 78X103795 : Col. G1 (version with cable ducts)
  Col. G2 (version for false floors)

3.4. - DESKIN AND COLLOCATION OF DSC 157

- Remove the front and rear DSC covers and panels.
- Remove the DSC from the wooden transport base.
- Release the orange coloured controller to cabinet fixing straps hence leave them routed on the cabinet (succesively replacing the blower grid) in such a way as not to impede swing - out of the electronics module.
- Place the DSC as per Site Layout Plans.
- Remove the nut and bolt that lock the ALI 260 swing-out panel

3.5. - DESKIN AND COLLOCATION OF DSU

3.5.1. - DSU 167

- Remove the unit panels and covers.
- Position the subsystem as per Site Layout Plans.
- Lower each spindle's stand-offs to prevent units from rolling. These stand-offs are capable of supporting the weight of the unit and may be used to level and/or align the drive.
- Open the top cover and remove all fixing hardware and packing material used for shipment (refer to fig. 3.1).
- Place the filter in the electronics fan module.
- Withold all those parts, utilized in the shipment, that are to be used for sub-system withdrawal operations.

3.5.2. - DSU 157 D

- Place the unit as per Site Layout Plans.
- Lower each spindle's stand-offs to prevent units from rolling.
- Remove the transparent cover blocks.
- Remove both front and rear panels.

- Extract all blocks, protection pads, etc. fitted on the unit during transport.

Note

Only remove the spindle protection cover and head protection block when ON-LINE operations are ready to be performed.
The head protection block may also be used as a special tool in case of particular operations that can be implemented whithout the dispac being loaded.

- Withold all those parts, used in the shipment, that are to be utilized for subsystem withdrawl operations.

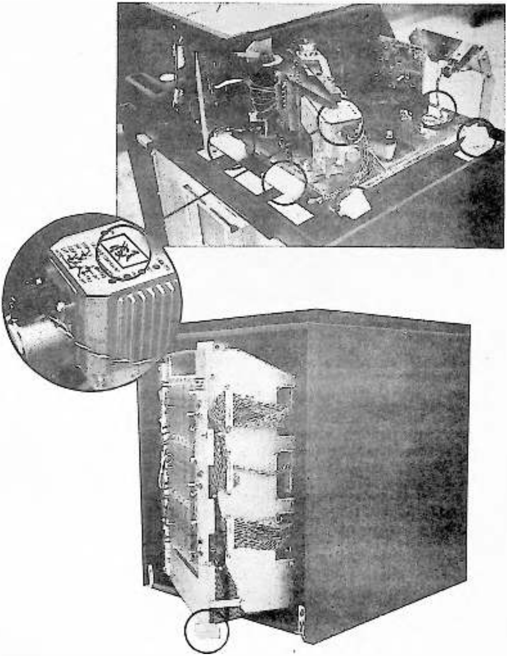


Fig. 3.1. - Fixing Hardware and Packing Material Locations

4. MECHANICAL ASSEMBLY

4.1. - CABLE DUCTS

- Draw out the cable duct to base elements from the DSS "Parts Kit" (Refer to P.L. 78X103795).
- Without tightening the screws, assemble them as per dwg. 78B103794(for version with cable ducts) or dwg. 78B103796 (for false floors).
- If the Site Layout Plans foresee a DSC to system connecting cable duct, assemble its elements as described for the DSS duct.

4.2. - DSS CABLE DUCTS ASSEMBLY

- Join the elements of the two cable ducts, tightening them starting from the CPU end.
- Fit the 2 connection elements (features 5 and 6 of Dwg. 78B103794)to the DSC cable output side of the duct.
- Locate the DSC near its pertinent duct and tighten in place.

4.3. - DSU ASSEMBLY

- Place the 1st disc drive near the cable duct (in false floor sites, the position of the 1st drive is only tied to the length of the cables).
- Screw in the 1st DSU stand-offs.
- Near all the following units to the first drive, screwing in all the pertinent stand-offs so as to bring them all to the same height.

Note

The stand-offs must only be turned the amount necessary to just lift the wheels off the floor and allow the AC cables to pass under them.

- When the levelling operations have been accomplished, tighten the stand-offs lock-nuts.

5. CABLE CONNECTIONS

Note

For cable layout, follow the identification tags on the cables themselves and dwgs 78B103828 (DSS) - 78C103857 (DSU 167) - C78106809 (DSU 157 D).
Should difficulties arise, in the interpretation of cable markings, refer to the documents attached to the machine documentation.
Dwgs 78B103830 (6/8m cables - 50/60 Hz), 78B103829 (2nd MPA), 78B103831 (MFS), 78B103858 (DSU 167), B78106808 (DSU 157 D).

5.1. - DSS INTERNAL CABLES

5.1.1. - Version with DSU 167s

- Draw out the 1st unit's cable Kit as per par. 3.3.2.
- Lay out and connect up the DSC to 1st unit cables following Dwgs 78B103828 and 78C103857.

- Take up any excess 1st unit cable, tidily wrapping and fixing it within the actual unit itself.

Note

To enable correct closure of the cable duct covers, follow the DSC to DSU's cable path layout illustrated in dwg. 78C103857.

- Draw out the relative cable Kits for each of the following units (see par. 3.3.2) and connect up.
- Take up any excess cable and fix it in the appropriate drive unit.
- Fit the TP 5 calibration plug on the last unit, as shown on dwg. 78C103857.

Note

The calibration plug is designated to the 1st DSU 167 but must always be placed on the last subsystem unit.

- Set the DSU breakers to OFF.

5.1.2. - Version with DSU 157 Ds

- Draw out the 1st DSU's cable kit as per par. 3.3.3.
- Lay out and connect up the DSC to 1st unit cables following dwgs. 78B103828 and C78106809.

Note

Cables within the unit and the DSC to DSU walkway trough must be layed out as illustrated in dwg. C78106809 to enable correct closure of the appropriate cables access hole, logics module and walkway cover.

- Draw out the cable kits specified in par. 3.3.3. for each of the units following the 1st DSU and appropriately connect them.
- Take up any excess cabling under the actual units themselves.
- Fit the TP 5 calibration plug on the last subsystem drive's J5 connector. Refer to dwg. C78106809.
- Set the DSUs a.c. breakers to OFF.

5.2. - DSS EXTERNAL CABLES

- Set the DSC breaker (ALI 260) to OFF.
- Draw out the pertinent cable Kit, as stated at para. 3.3.1.
- Lay out these cables with the symbolic marking side (i.e. L-DSS-A) either towards the CPU or the MPA (see USC forms) and check the integrity of the markings on both cable ends.
- Remove the ALI 260's front cover plate.
- Connect cables C1 to C9 following the instructions contained in the USC forms and respecting the markings on the cables themselves. Fix the cables on the ALI 260 with the aid of the appropriate Bushing type pliers. Refer to fig. 5.1.
- Place the a.c. input cable in the appropriate ALI 260 connector.

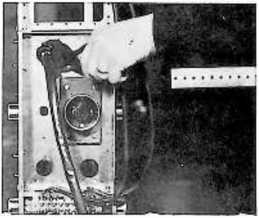


Fig. 5.1. - Use of the Bushing Pliers

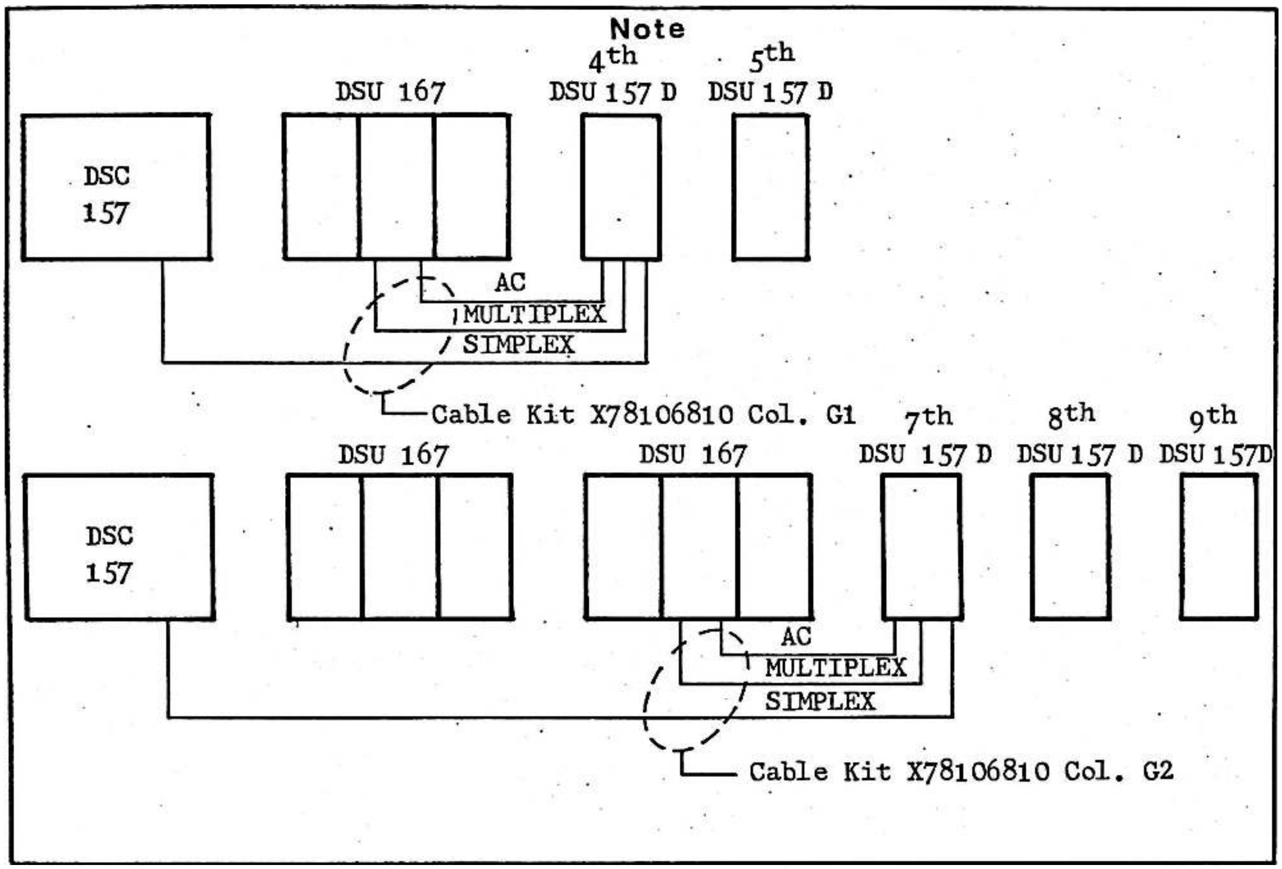
5.3. - DSS ADD-ONS

5.3.1. - Homogeneous DSU Add-Ons

- When DSS 157 add-ons are to be installed, should these be the same type of drives as already present in the Site, all requirements specified in par. 5.1. hold true.
- Move the calibration plug on the last unit's J5 connector before starting to connect up the cables.

5.3.2. - DSU 157 D Add-Ons In DSS 157 Subsystem With DSU 167s

- Part numbers of the cable kits required to connect the DSU 157 Ds that follow the 1st DSU 167 (cable kit Col. G1) and the 2nd DSU 167 (cable kit Col. G2) are shown on P.L. X78106810.



- For all tie-up requirements refer to par. 5.1.1., 5.1.2. and dwg. 78C103857 and C78106809.
- Cable kits for units that follow the connecting drive are the same as those outlined in par. 3.3.3.

6. VISUAL CHECKS

6.1. - DSU 167

> **Note**
> The following operations are to be carried out on every spindle

- Set the logics' and Power Supply's breakers to OFF.
- Clean the spindle and shroud with disc cleaner.
- Check and clean the read/write heads.
- Install a dispac on the drive
- Manually move the brush holder into the dispac, checking visually that the holder does not contact the edges of the dispac.
- Manually retract the brush holder until it catches in position.
- Release the head loading latch on the carriage and manually disengage the detent from the detent gear.
- Manually move the carriage forward slowly, be sure that all the heads, leaf springs and leadwires result clear off the edges of the discs.
- Move the carriage back to its original position.
- Check that no oil leaks-out.

6.2. - DSU 157 D

- Set the main a.c. breaker to OFF and the remaining breakers to ON (Power Supply and Sequence Box).
- Set maintenance panel switches ON-LINE, LOGIC and SERVO to the OFF position and verify that the other panel switches are down.
- Remove the heads protector block and the spindle protection cover.
- Inspect and clean the heads.
- Clean both the shroud and the spindle.
- Ascertain that carriage, index group and brushes are in the fully retracted position.
- Load a scratch dispac on the unit.

- Manually push the brush arm into the pac and insure that no interference occurs on the disc surfaces.
- Retract the brush arm.
- Manually release the head loading lever latch and move the carriage forward.

Note

With the latch released, the head loading lever is always raised to impede heads from loading.

- Check that the heads, leadwires and leaf springs result clear off the edges of the discs.
- In these conditions, also verify that the carriage does not present any binds or hard spots.
- Fully retract the carriage,detenting the head loading lever.
- Remove the scratch dispac.

7. CHECK–OUT

7.1. – OFF–LINE CHECKS

7.1.1. – DSC

- Set the AC input breakers to ON (ALI 260 on DSC).
- Check that all the DSC logics module fans rotate freely and blow air upwards. If this is not the case, check for correct phase connections.
- Check that adjustment and transformer module fans blow air onto their relative modules.

7.1.2. – DSU 167

- Turn power ON at the Power Supply and logics module.
- Set operator panel Start–Stop switch to Start.
- Check for counterclokwise rotation of the dispac. Should all 3 spindles rotate wrongly, swap two DSU a.c. phases on the DSC's ALI 260.

7.1.3. – DSU 157 D

- Set main a.c. breaker and maintenance panel LOGIC switch to ON.
- Observe that both the STOP and LOAD indicators, on the operator panel, are illuminated.

Note

Should both START and STOP indicators be lit, depress START and verify that only the STOP indicator remains illuminated.

Should the STOP and LOAD indicators not light–up, check the safety interlocks circuit.

- Insure that the index lamp is lit.
- Observe that the PHASE SEQ lamp is off.

Note

Should this lamp be bit on all the subsystem's DSU 157 Ds, interchange two phases within the DSC's ALI 260.
If, on the other hand, the PHASE SEQ lamp is only lit on one unit, proceed to check for the fault in either the unit's "AC Box" or "Sequence Box".

- Verify that the TEMP lamp is off and that all 5 fans rotate.
- Set maintenance panel SERVO switch to OFF.
- Load a scratch dispac on the unit, depress START and verify that :
  - . START lamp illuminates
  - . Lamps LOAD and STOP turn off
  - . Glass cover is secured
  - . The dispac rotates counterclockwise
  - . Cleaning brushes cycle is completed.
- Depress STOP and check for the following events :
  - . STOP indicator lights-up
  - . Pac halts after approx. 12 secs.
  - . LOAD indicator lights enabling to now open the glass cover.
- Set maintenance panel SERVO and ON-LINE switches ON and depress START. Ascertain that the heads are loaded correctly and that the READY indicator turns on.
- Switch the unit off and replace the covers.
- Repeat all the described operations on each DSU 157 D.

7.2. - ON-LINE CHECKS

Note

Dispacs used for the tests must first be cleaned and held stored in the site environment for at least 2 hours.

- These checks, implemented through diagnostic programs, are only to be carried out after the CPU and program loading subsystem final check-out operations have been accomplished.
- Check that the held diagnostics correspond to the DSC 157 documentation given on dwg. 74A104859 attached to the DSC 157 documentation.

7.2.1. - Sequence of Operations

- Sequentially feed through the below listed subsystem diagnostics, following the indication given in the pertinent descriptions :
  - Automatic Isolation Test (on 1 spindle only)
  - Functional Test (on 2 spindles) after due formatting of discs.
  - Unit Margining Test (on all connected unit spindles using ONE FORMATED DISC ONLY - compatibility test).

Note

Possible errors given by a single spindle can be traced with the aid of the appropriate Maintenance Aids that are inserted in the DSU 167 or DSU 157 D Maintenance Manuals.

8. FINAL OPERATIONS

8.1. - SKIN-UP

- Set the a.c. input breaker to OFF (ALI 260 on DSC).
- Check that drive unit model, serial number and product code, on the yellow label, correspond to the description given on the Product Composition Sheet.
- Replace all panels and covers removed at the beginning of the installation procedures. See par.3.4 , 3.5 and 5.2.
- Fit the cable ducts covers (walkways) making sure that the underlying cables will not be crimped or chafed.
- Set the a.c. input breaker to ON.

8.2. - CHECKS AFTER HANDOVER TO CUSTOMER

- Check that the supplied tools and equipment correspond to the pertinent packing list.
- Prepare a report giving details of snags or defects found during the installation and / or commissioning. Should it be the case that such inconveniences be found on the DSU 167s, specify the involved spindle.
- Fill-in the possible "Surveillance Plan" or other special analysis plans as required.

9. SUBSYSTEM WITHDRAWAL

When a subsystem is withdrawn from a site, it must be packed complete of all cable and part Kits originally consigned.
Particular attention is to be made to the following requirements :

- The first DSU 167 must have a cable kit as per P.L. 78X103856 (Col. G1).
- Each DSU 167 following the 1st unit must be complete of a cable Kit as per P.L. 78X1003856 (Col. G2-G3).
- The controller must be complete of a cable kit and part kit as indicated on P.Ls. 78X103827 and 78X103795 respectively.
- Each DSU 157 D must be complete of a cable kit as per P.L. X78106807 (Col. G1-G8) and/or P.L. X78106810 (Col. G1-G2).
- Connecting cable ducts and walkways must be packed in a separate crate.

9.1. - REMOVAL

Sequentially carry out the following operations:

- Remove all power from the system.
- Remove all the cable duct covers (walkways).
- Remove both the rear and front panels from each unit.
- Disconnet the system connecting cables.
- Group the above mentioned cables and identify the bundle with the same kit P/N given on P.L. 78X103827 (col. G1 to G8).
- Disconnect all cables going to the units, from the DSC side.
- Disconnect the same cables plus those going towards the 2nd unit, from the 1st unit side.
- Proceed as above for all the following units.
- Remove the terminator plug located on the last unit.

Carry out the following operations on each physical unit.

9.1.1. - DSU 167

- Lock the logics panel.
- Immobilize the carriage with its pertinent tie wire.
- Cover the valve hole on the actuator assembly with the appropriate plug, fixing this latter with adhesive tape (fig. 3.1.).
- Immobilize the main deck with the pertinent wedges (Refer to fig. 3.1).
- Lift the stand-offs allowing the unit to be moved.
- Replace all the panels.

9.1.2. - DSU 157 D

- Lock the logics panel.
- Immobilize the carriage with its appropriate tie-wire
- Fit the pertinent heads protector block and spindle cone protection cover.
- Secure the glass cover.
- Raise the stand-offs allowing the units to moved on their wheels.
- Replace all covers and panels.

9.1.3. - DSC 157

- Lock the electronics swing-out module with the appropriate orange coloured fixing straps.
- Secure the ALI 260 module with the pertinent nut and bolt.
- Skin-up the controller.
- Group all the DSS to CPU connecting cable ducts (walkways) and set them aside.
- Finally disassemble all the cable ducts witholding all fixing hardware.

9.2. - WITHDRAWAL

The units' making up the subsystem and the pertinent Kits, must satisfy the following requirements:

1) - The DSC 157 must comprise:

- Part Kits
- Cable Kits

- Subsystem documentation (vol. 1 to 8F).
- Diagnostic decks
- All non implemented FCOs
- The specific tools.

2) – Each DSU 167 and DSU 157 D must comprise :

- Cable Kits
- Machine documentation
- All non implemented FCOs
- The specific tools.

3) – Tidily set aside, the connecting cable ducts (walkways) must be complete of all their relative fixing hardware.

10. ATTACHED DRAWINGS

To complete this manual, the following drawings and part lists have been attached:

DESCRIPTION	PART LIST or DWG. No.	SHEETS
DSS Cable Markings and Connections (6-8m cables)	78B103830	
DSS Cable Markings and Connections (2nd MPA)	78B103829	
DSS Cable Markings and Connections (MPS)	78B103831	
DSS Cable Installation Layout	78B103828	2
DSS Cable Kits	78X103827	2
Parts Installation Layout (version with cable ducts)	78B103794	
Parts Installation Layout (false floor sites)	78B103796	
DSS Part Kits	78X103795	2
DSS 167 Cable Markings and Connections	78B103858	
DSU 167 Cable Installation Layout	78C103857	
DSU 167 Cable Kits	78X103856	
DSU 157 D Cable Markings and Connections	B78106808	3
DSU 157 D Cable Installation Layout	C78106809	
DSU 157 D Cable Kits	X78106807	3
Mixed DSUs (167 and 157 D) Cable Markings and Connections	B78106811	
Mixed DSUs (167 and 157 D) Cable Kits	X78106810	

78B103830

REVISIONI					
REV	ORD. APPL.	DATA A	DATA M	DATA G	FIRMA
A	CO M100827	71	03	16	Alberti

Δ1	RIF. REF.	TIPO TYPE	Δ2 G1	G2	G3	G4	MARCATURA E COLLEGAMENTO CAVI CABLE CONNECTION AND MARKING Δ3 — LATO INT. ALL' U.F. SIDE INT. TO PH. UNIT	LATO EST. ALL' U.F. SIDE EST. TO PH.UNIT	FUNZ. FUNCT.	NOTE NOTES
	C1	NS107	1	10	1	10	DSC157-GUD040-J1	L-DSS-A	LOG.	Δ12
								L-DSS-B		Δ13
	C2	NS107	1	10	1	10	DSC157-GUD040-J2	L-DSS-C	LOG.	Δ12
								L-DSS-D		Δ13
	C3	NS113	2	11	2	11	DSC157-GUD040-J3	L-DSS-E	LOG.	
	C4	AL100	3	12	3	12	DSC157-GUD040-P4	U-DSS-+20	D.C.	Δ4
	C5	AL101	4	13	4	13	DSC157-GUD040-P2	U-DSS-MASSA	D.C.	Δ5
	C6	AL146	5	14			DSC157-ALI260-J1	DSS-A.C.-INPUT	A.C.	
	C6	AL145			19	20	DSC157-ALI260-J1	DSS-A.C.-INPUT	A.C.	
	C7	AL125	6	15	6	15	DSC157-ALI260-P5-1	P-DSS-3	CONTR.	Δ8
							2	4		Δ4
							3	5		Δ4
	C8	AL141	7	16	7	16	DSC157-ALI260-P5-1	P-DSS-3	CONTR.	Δ8
							4	1		Δ5
							5	2		Δ4
	C9	AL141	8	17	8	17	DSC157-VAR585-P20a-1	V-DSS-7	CONTR.	Δ8
							2	8		Δ4
							3	9		Δ5
X	P1		9	9	9	9	ALI 260-P5-7	ALI 260-P5-8	CONTR.	Δ1
X	P2		9	9	9	9	ALI 260-P5-4	ALI 260-P5-5	CONTR.	Δ1
X	P3		9	9	9	9	ALI 260-P5-5	ALI 260-P5-6	CONTR.	Δ1

FOR THE CABLES ASSEMBLY SIDE REF. TO DRAW No 78B103828	PER IL MONTAGGIO CAVI VEDI DIS. 78B103828
Δ13 - CONNECTOR 2 OF THE CABLE	Δ13 - CONNETTORE 2 DEL CAVO
Δ12 - CONNECTOR 1 OF THE CABLE	Δ12 - CONNETTORE 1 DEL CAVO
Δ11 _ YELLOW-GREEN	Δ11 _ GIALLO-VERDE
Δ10 - WHITE	Δ10 - BIANCO
Δ9 - GREEN	Δ9 - VERDE
Δ8 - BROWN	Δ8 - MARRONE
Δ7 - BLUE	Δ7 - BLU
Δ6 - RED	Δ6 - ROSSO
Δ5 - BLACK	Δ5 - NERO
Δ4 - YELLOW	Δ4 - GIALLO
Δ3 - SEE LABELLING INSTRUCTION DRAWING No 09874 010	Δ3 - VEDERE ISTRUZ. MARCATURA DIS No 09874 010
Δ2 - ITEM NUMBERS SHOWN APPLY TO DRAWING No 78X103827	Δ2 - PARTI NUMERATE SECONDO LISTA DIS 78X103827
Δ1-X - PARTS ASSEMBLED WHEN DELIVERED	Δ1-X - PARTI MONTATE ALLA SPEDIZIONE
NOTES	NOTE

SALVO INDICAZIONE CONTRARIA DIMENSIONI: MILLIMETRI / INCH TOLLERANZE DIMENS. E DI FORMA VEDI: PROIEZIONE	MAT.	**Honeywell** Honeywell Information Systems Italia
	TT.	DESCRIZIONE 6-8 MT. MARCAT. E COLLEG. CAVI
	FIN.	DISEGNO 78B103830
SCALA	COD.	FAG 1/1
	DISEGNATO	REV A
	APPROVATO	
	DISTR.	

Mod. 1153

78B103829

REVISIONI					
REV	ORD. APPL.	DATA			FIRMA
		A	M	G	
A	CO M100827	71	03	16	Alberti P.

△1	RIF. REF.	TIPO TYPE	△2		MARCATURA E COLLEGAMENTO CAVI, CABLE CONNECTION AND MARKING △3		FUNZ. FUNCT.	NOTE NOTES
			G5	G6	LATO INT. ALL' U.F. SIDE INT TO PH. UNIT	LATO EST. ALL' U.F. SIDE EST. TO PH.UNIT		
	C1	NS107	1	1	DSC 157 - GUD 040 - J1	L - DSS - A	LOG.	△12
						L - DSS - B		△13
	C2	NS 107	1	1	DSC 157 - GUD 040 - J2	L - DSS - C		△12
						L - DSS - D		△13
	C3	NS113	2	2	DSC 157 - GUD 040 - J3	L - DSS - E	LOG.	
	C4	AL100	21	21	DSC 157 - GUD 040 - P4	U - DSS - +20	D.C.	△4
	C5	AL101	22	22	DSC 157 - GUD 040 - P2	U - DSS - MASSA	D.C.	△5
	C6	AL146	23		DSC157 - ALI 260 - J1	DSS - A.C. - INPUT	A.C.	
	C6	AL145		26	DSC157 - ALI 260 - J1	DSS - A.C. - INPUT	A.C.	
	C7	AL125	24	24	DSC 157 - ALI 260 - P5 - 1	P - DSS - 3	CONTR.	△8
					2	4		△4
					3	5		△4
	C8	AL141	25	25	DSC 157 - ALI 260 - P5 - 1	P - DSS - 3	CONTR.	△8
					4	1		△5
					3	2		△4
	C9	AL141	25	25	DSC 157 - YAR585 - P202 - 1	V - DSS - 7	CONTR.	△8
					2	8		△4
					3	9		△5
X	P1		9	9	ALI 260 - P5 - 7	ALI 260 - P5 - 8	CONTR.	△1
X	P2		9	9	ALI 260 - P5 - 4	ALI 260 - P5 - 5	CONTR.	△1
X	P3		9	9	ALI 260 - P5 - 5	ALI 260 - P5 - 6	CONTR.	△1

FOR THE CABLES ASSEMBLY
SIDE REF. TO DRAW. No. 78B103828

△13 - CONNECTOR 2 OF THE CABLE

△12 - CONNECTOR 1 OF THE CABLE

△11 - YELLOW-GREEN
△10 - WHITE
△9 - GREEN
△8 - BROWN
△7 - BLUE
△6 - RED
△5 - BLACK
△4 - YELLOW

△3 - SEE LABELLING INSTRUCTION
DRAWING No 09874 010

△2 - ITEM NUMBERS SHOWN APPLY TO
DRAWING N. 78X103827

△1-X - PARTS ASSEMBLED
WHEN DELIVERED

NOTES

PER IL MONTAGGIO CAVI
VEDI DIS. 78B103828

△13 - CONNETTORE 2 DEL CAVO

△12 - CONNETTORE 1 DEL CAVO

△11 - GIALLO-VERDE
△10 - BIANCO
△9 - VERDE
△8 - MARRONE
△7 - BLU
△6 - ROSSO
△5 - NERO
△4 - GIALLO

△3 - VEDERE ISTRUZ. MARCATURA
DIS. No 09874 010

△2 - PARTI NUMERATE SECONDO
LISTA DIS 78X103827

△1-X - PARTI MONTATE ALLA
SPEDIZIONE

NOTE

SALVO INDICAZIONE CONTRARIA
DIMENSIONI: MILLIMETRI / INCH
TOLLERANZE DIMENS. E DI FORMA VEDI:
PROIEZIONE
SCALA
COD.

MAT.
TT..
FIN.
DISEGNATO
APPROVATO
DISTR.

Honeywell
Honeywell Information Systems Italia

DESCRIZIONE II MPA
MARCAT. E COLLEG. CAVI

DISEGNO 78B103829
PAG 1/1
REV A

Mod 1153

78B103831

REVISIONI					
REV	ORD. APPL.	DATA A	DATA M	DATA G	FIRMA
A	CO M100827	71	03	16	Alberti P.

MARCATURA E COLLEGAMENTO CAVI
CABLE CONNECTION AND MARKING △3

△1	RIF. REF.	TIPO TYPE	△2 G7	△2 G8	LATO INT. ALL' U.F. SIDE INT. TO PH. UNIT	LATO EST. ALL' U.F. SIDE EST. TO PH.UNIT	FUNZ. FUNCT.	NOTE NOTES
	C1- (1)	NS154	28	28	DSC157-GUD040-J1	LC-DSS-AEB	LOG.	△
	(2)				J3			△
	C2	NS153	29	29	DSC157-GUD040-J2	LC-DSS-DAC	LOG.	△
	C4	AL100	3	3	DSC157-GUD040-P4	UC-DSS-+20	D.C.	△4
	C5	AL101	4	4	DSC157-GUD040-P2	UC-DSS-MASSA	D.C.	△5
	C6	AL146	5		DSC157-ALI260-J1	DSS-AC-INPUT	A.C.	
	C6	AL145		19	DSC157-ALI260-J1	DSS-AC-INPUT	A.C.	
	C7	AL204	30	30	DSC157-ALI260-P5-1	PC-DSS-ON	CONTR.	△8
					2			△4
					3			△4
	C8	AL204	30	30	DSC157-ALI260-P5-1	PC-DSS-24	CONTR.	△
					4			△
					3			△4
	C9	AL204	30	30	DSC157-VAR585-P90-1	PC-DSS-CONT	CONTR.	△
					2			△
					3			△5
x	P1		9	9	ALI260-P5-7	ALI260-P5-8	CONTR.	△1
x	P2		9	9	ALI260-P5-4	ALI260-P5-5	CONTR.	△1
x	P3		9	9	ALI260-P5-5	ALI260-P5-6	CONTR.	△1

FOR THE CABLES ASSEMBLY SIDE REF. TO DRAW No 78B103828	PER IL MONTAGGIO CAVI VEDI DIS. 78B103828
△13 - CONNECTOR 2 OF THE CABLE	△13 - CONNETTORE 2 DEL CAVO
△12 - CONNECTOR 1 OF THE CABLE	△12 - CONNETTORE 1 DEL CAVO
△11 - YELLOW-GREEN	△11 - GIALLO-VERDE
△10 - WHITE	△10 - BIANCO
△9 - GREEN	△9 - VERDE
△8 - BROWN	△8 - MARRONE
△7 - BLUE	△7 - BLU
△6 - RED	△6 - ROSSO
△5 - BLACK	△5 - NERO
△4 - YELLOW	△4 - GIALLO
△3 - SEE LABELLING INSTRUCTION DRAWING No 09874 010	△3 - VEDERE ISTRUZ. MARCATURA DIS. No 09874 010
△2 - ITEM NUMBERS SHOWN APPLY TO DRAWING No 78X103827	△2 - PARTI NUMERATE SECONDO LISTA DIS. 78X103827
△1-X - PARTS ASSEMBLED WHEN DELIVERED	△1-X - PARTI MONTATE ALLA SPEDIZIONE
NOTES	NOTE

SALVO INDICAZIONE CONTRARIA
DIMENSIONI: MILLIMETRI / INCH
TOLLERANZE DIMENS. E DI FORMA VEDI:
PROIEZIONE
SCALA
COD.
MAT.
TT.
FIN.
DISEGNATO
APPROVATO
DISTR.

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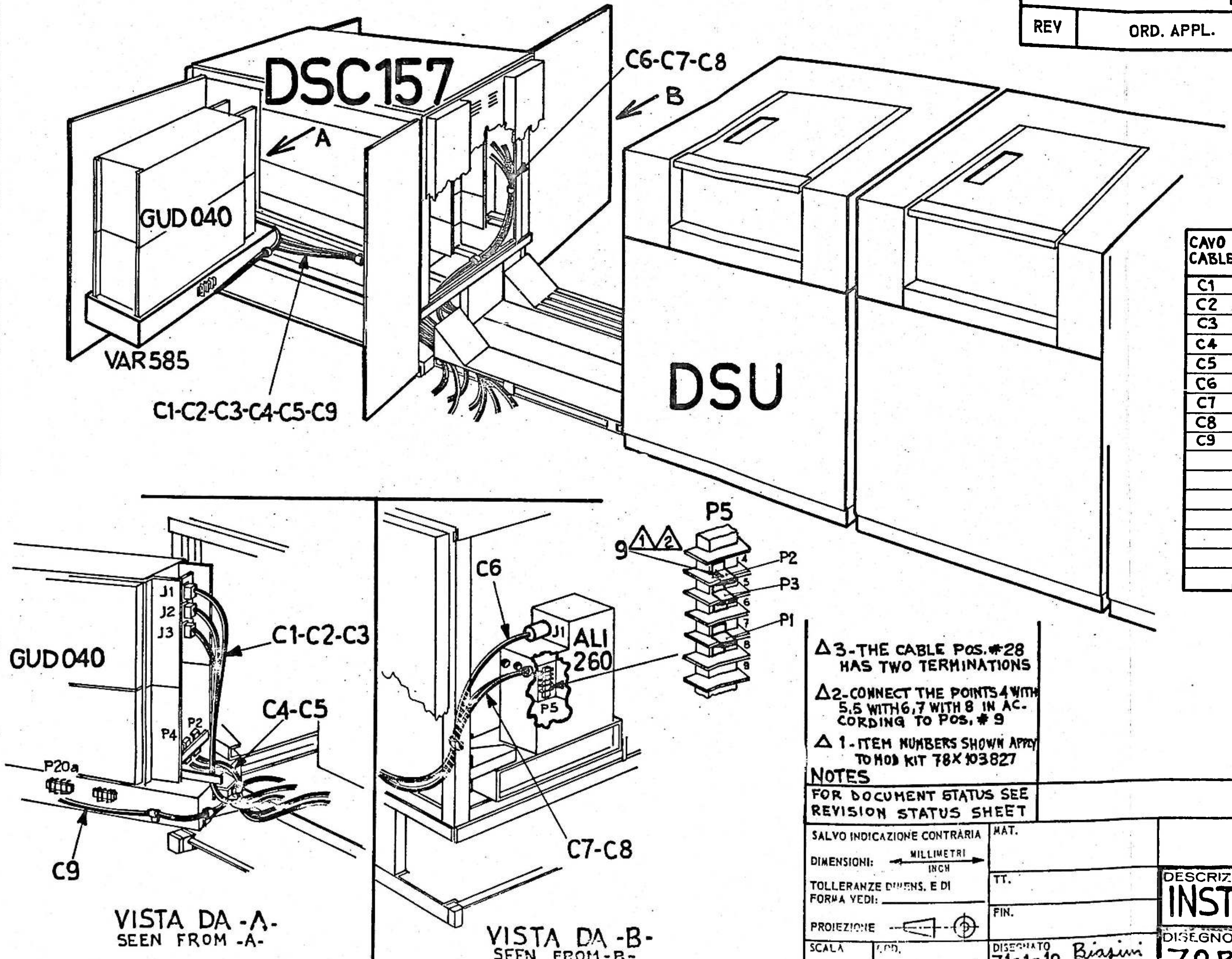
Honeywell Information Systems Italia

DESCRIZIONE MPS
MARCAT. E COLLEG. CAVI

DISEGNO 78B103831
PAG 1/1
REV A

78B103828

REVISIONI					
REV	ORD. APPL.	DATA A	DATA M	DATA G	FIRMA



CAVO CABLE	G1	G2	G3	G4 △1	G5	G6	G7 △3	G8 △3
C1	1	10	1	10	1	1	28	28
C2	1	10	1	10	1	1	29	29
C3	2	11	2	11	2	2	/	/
C4	3	12	3	12	21	21	3	3
C5	4	13	4	13	22	22	4	4
C6	5	14	19	20	23	26	5	19
C7	6	15	6	15	24	24	30	30
C8	7	16	7	16	25	25	30	30
C9	8	17	8	17	25	25	30	30

△3-THE CABLE POS. #28 HAS TWO TERMINATIONS

△2-CONNECT THE POINTS 4 WITH 5, 5 WITH 6, 7 WITH 8 IN ACCORDING TO POS. # 9

△1-ITEM NUMBERS SHOWN APPLY TO MOD KIT 78X103827

NOTES

FOR DOCUMENT STATUS SEE REVISION STATUS SHEET

△3-IL CAVO A POS. N° 28 HA DUE TERMINAZIONI

△2-PONTICELLARE I CONTATTI 4 CON 5 : 5 CON 6 : 7 CON 8 CON PONTICELLI A POS. N° 9

△1-PARTI NUMERATE SECONDO LISTA N° 78X103827 (NELLA COLONNA POS. N°)

NOTE

PER IL LIVELLO DI MODIFICA VEDI FOGLIO REVISIONI

SALVO INDICAZIONE CONTRARIA

DIMENSIONI: MILLIMETRI / INCH

TOLLERANZE DIMENS. E DI FORMA VEDI:

PROIEZIONE

SCALA

COD.

MAT.

TT.

FIN.

DISEGNATO 71-1-10 Biasini

APPROVATO

DISTR.

Honeywell

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DESCRIZIONE VERS. CON PEDANE

INSTALLAZ. CAVI

DISEGNO 78B103828

PAG 1/2

REV A

S.T.

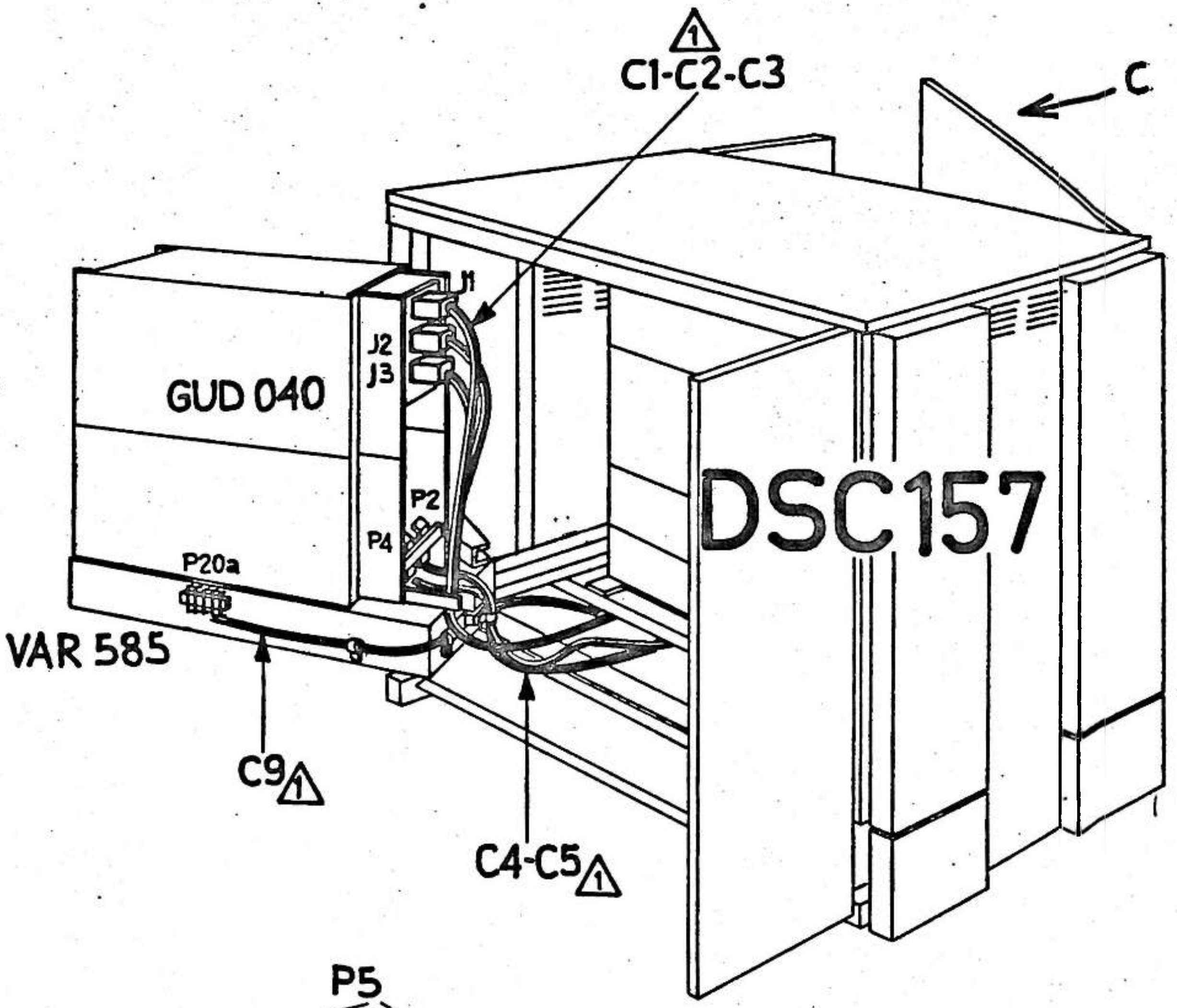
Cod. 3896104 Q

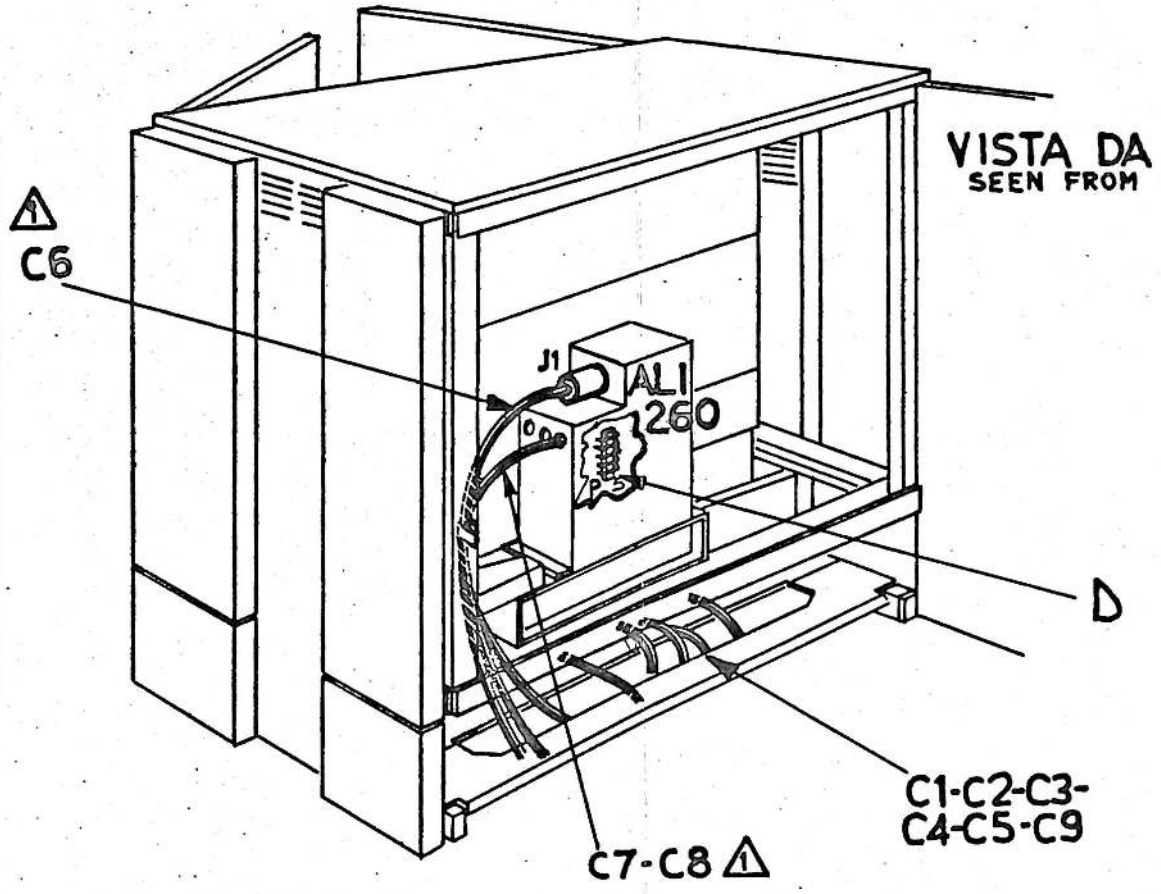
63 10 30

78B103828

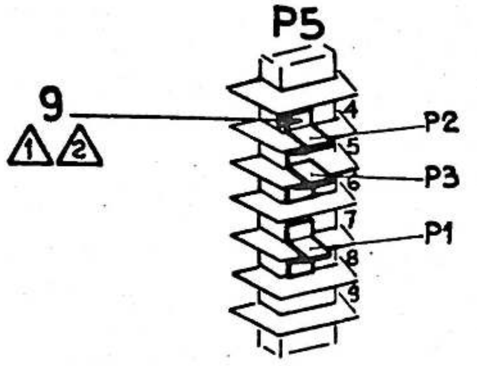
REV	ORD. APPL.	DATA A	DATA M	DATA G	FIRMA

REVISIONI





VISTA DA -C-
SEEN FROM -C-



VISTA DA -D-
SEEN FROM -D-

THE RELATIVE POSITION BETWEEN DSU AND DSC IS NOT DEFINED, LIMITED ONLY BY CABLES LENGTH.

NOTES

NON E' DEFINITA LA POSIZIONE RELATIVA TRA DSU E DSC, LIMITATA SOLO DALLA LUNGHEZZA DEI CAVI.

NOTE

SALVO INDICAZIONE CONTRARIA
DIMENSIONI: MILLIMETRI / INCH
TOLLERANZE DIMENS. E DI FORMA VEDI:
PROIEZIONE
SCALA
COD.

MAT.
TT.
FIN.
DISEGNATO 71-GEN. 12 Biasini
APPROVATO
DISTR.

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DESCRIZIONE VERSIONE DOPPIO PAVIMENTO
INSTALLAZ. CAVI
DISEGNO 78B103828
PAG 2F
REV A

S.T.

Cod. 3898104 Q

69 10 30

CODICE			
G1	0643457K	G5	0643461B
G2	0643458G	G6	0643462P
G3	0643459C	G7	0643463K
G4	0643460A	G8	0643464G

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PL 78X103827 PAG. 1/2 REV.

*	POS. NO	CD	NUMERO DI IDENTIFICAZIONE	DESCRIZIONE DELLA PARTE		GRUPPI E QUANTITA' G1	G2	G3	G4	G5	G6	G7	G8	UM
	1	0	78X104172G2	CAVO NS107	0640145K	2		2		2	2			EA
	2	0	78A104200G4	CAVO NS113	0640069V	1		1		1	1			EA
	3	0	78X104123G7	CAVO AL100	0640390J	1		1				1	1	EA
	4	0	78X104120G6	CAVO AL101	0640327V	1		1				1	1	EA
	5	0	78A104206G5	CAVO AL146	0640749Y	1						1		EA
	6	0	78X104203G3	CAVO AL125	0640530Y	1		1						EA
	7	0	78X104064G1	CAVO AL141	0640613H	1		1						EA
	8	0	78X104063G6	CAVO AL141	0640856X	1		1						EA
	9	1	5612920U	PONTICELLO	5612920U	3	3	3	3	3	3	3	3	EA
	10	0	78X104171G8	CAVO NS107	0640026C		2		2					EA
	11	0	78A104200G3	CAVO NS113	0640066G		1		1					EA
	12	C	78X104123G5	CAVO AL 100	0640397U		1		1					EA
	13	0	78X104120G4	CAVO AL 101	0640351P		1		1					EA
	14	0	78A104206G4	CAVO AL 146	0640857T		1							EA
	15	0	78X104203G4	CAVO AL 125	0640525Z		1		1					EA
	16	C	78X104063G7	CAVO AL 141	0640614W		1		1					EA

S.T.

CD - CODICE DI DISEGNO
0 - DISEGNO ISG
1 - PARTE ACQUISTATA A CATALOGO
2 - RICHIAMO DI PIU' ALTERNATIVE
3 - PARTE A CATALOGO DA MODIFICARE
4 - PARTE ISG DA MODIFICARE
5 - PARTE DA SELEZIONARE

UM - UNITA' DI MISURA
EA
✗ - NUMERO
IN - INCH
G - GRAMMO
CM - CENTIMETRO

✱ ULTIME POSIZIONI MODIFICATE

DESCRIZIONE
KIT CAVI DSS 157

PL 78X103827 PAG. 1/2 REV. A1

PER LE MODIFICHE VEDI FOGLIO REVISIONE

Cod 3896111G 68 10 30

Honeywell
Honeywell Information Systems Italia

PL 78X103827 PAG. 2/F REV.

*	POS. NO	CD	NUMERO DI IDENTIFICAZIONE	DESCRIZIONE DELLA PARTE		GRUPPI E QUANTITA' G1	G2	G3	G4	G5	G6	G7	G8	UM
	17	0	78X104063G3	CAVO AL 141	0640548Y		1		1					EA
	18	0	78B103830	MARCAT. E COLL. CAVI		X	X	X	X					.
	19	0	78A104205G5	CAVO AL 145	0640860J			1						EA
	20	0	78A104205G4	CAVO AL 145	0640645V				1				1	EA
	21	0	78X104123G8	CAVO AL 100	0640387B					1	1			EA
	22	0	78X104120G7	CAVO AL 101	0640386F					1	1			EA
	23	0	78A104206G6	CAVO AL 146	0640746B					1				EA
	24	0	78X104203G5	CAVO AL 125	0640537A					1	1			EA
	25	0	78X104064G4	CAVO AL 141	0640611Z					2	2			EA
	26	0	78A104205G6	CAVO AL 145	0640747F						1			EA
	27	0	78B103829	MARCAT. E COLL. CAVI						X	X			
	28	0	78A100608G1	CAVO NS 154	0640200V							1	1	EA
	29	0	78A100609G1	CAVO NS 153	0640197G							1	1	EA
	30	0	78A100592G1	CAVO AL 204	0640962Z							3	3	EA
	31	0	78B103831	MARCAT. E COLL. CAVI								X	X	
	32	0	78B103828	INSTALLAZ. CAVI		X	X	X	X	X	X	X	X	

S.T.

CD - CODICE DI DISEGNO
0 - DISEGNO ISG
1 - PARTE ACQUISTATA A CATALOGO
2 - RICHIAMO DI PIU' ALTERNATIVE
3 - PARTE A CATALOGO DA MODIFICARE
4 - PARTE ISG DA MODIFICARE
5 - PARTE DA SELEZIONARE

UM - UNITA' DI MISURA
EA
✗ - NUMERO
IN - INCH
G - GRAMMO
CM - CENTIMETRO

✱ ULTIME POSIZIONI MODIFICATE

DESCRIZIONE
KIT CAVI DSS 157

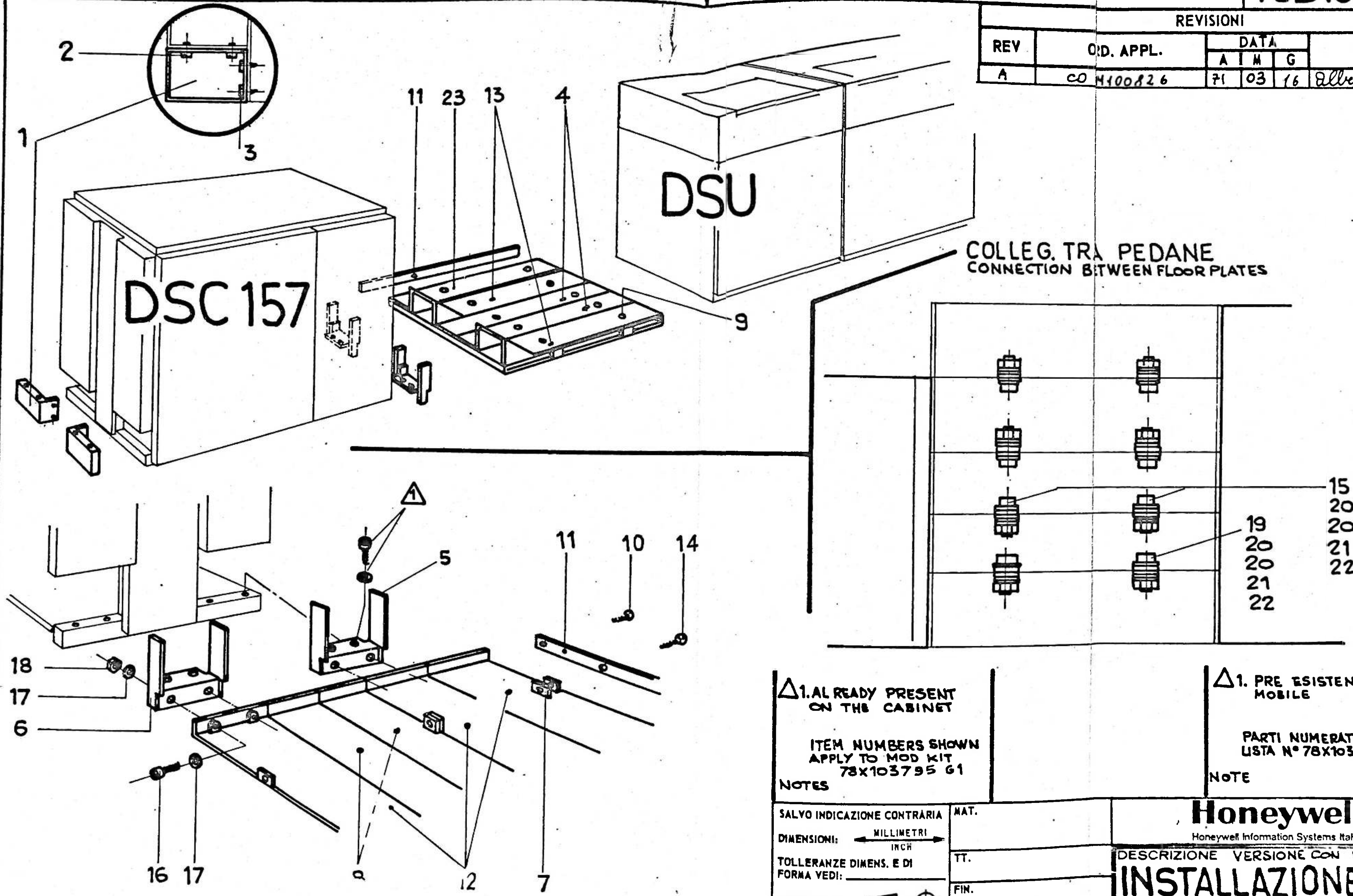
PL 78X103827 PAG. 2F REV. A1

PER LE MODIFICHE VEDI FOGLIO REVISIONE

Cod 3896111G 68 10 30

78B103794

REVISIONI					
REV	O.D. APPL.	DATA A	DATA M	DATA G	FIRMA
A	CO H100826	71	03	16	Alberti P.



△1. ALREADY PRESENT ON THE CABINET

ITEM NUMBERS SHOWN APPLY TO MOD KIT 78X103795 G1

NOTES

△1. PRE ESISTENTI SUL MOBILE

PARTI NUMERATE SECONDO LISTA N° 78X103795 G1

NOTE

SALVO INDICAZIONE CONTRARIA
DIMENSIONI: MILLIMETRI / INCH
TOLLERANZE DIMENS. E DI FORMA VEDI:
PROIEZIONE
SCALA
COD.
MAT.
TT.
FIN.
DISEGNATO 30 DIC. 70 Cecchini Sebastiano
APPROVATO
DISTR.

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Honeywell Information Systems Italia

DESCRIZIONE VERSIONE CON PEDANE
INSTALLAZIONE PARTI

DISEGNO 78B103794
PAG 1/1
REV A

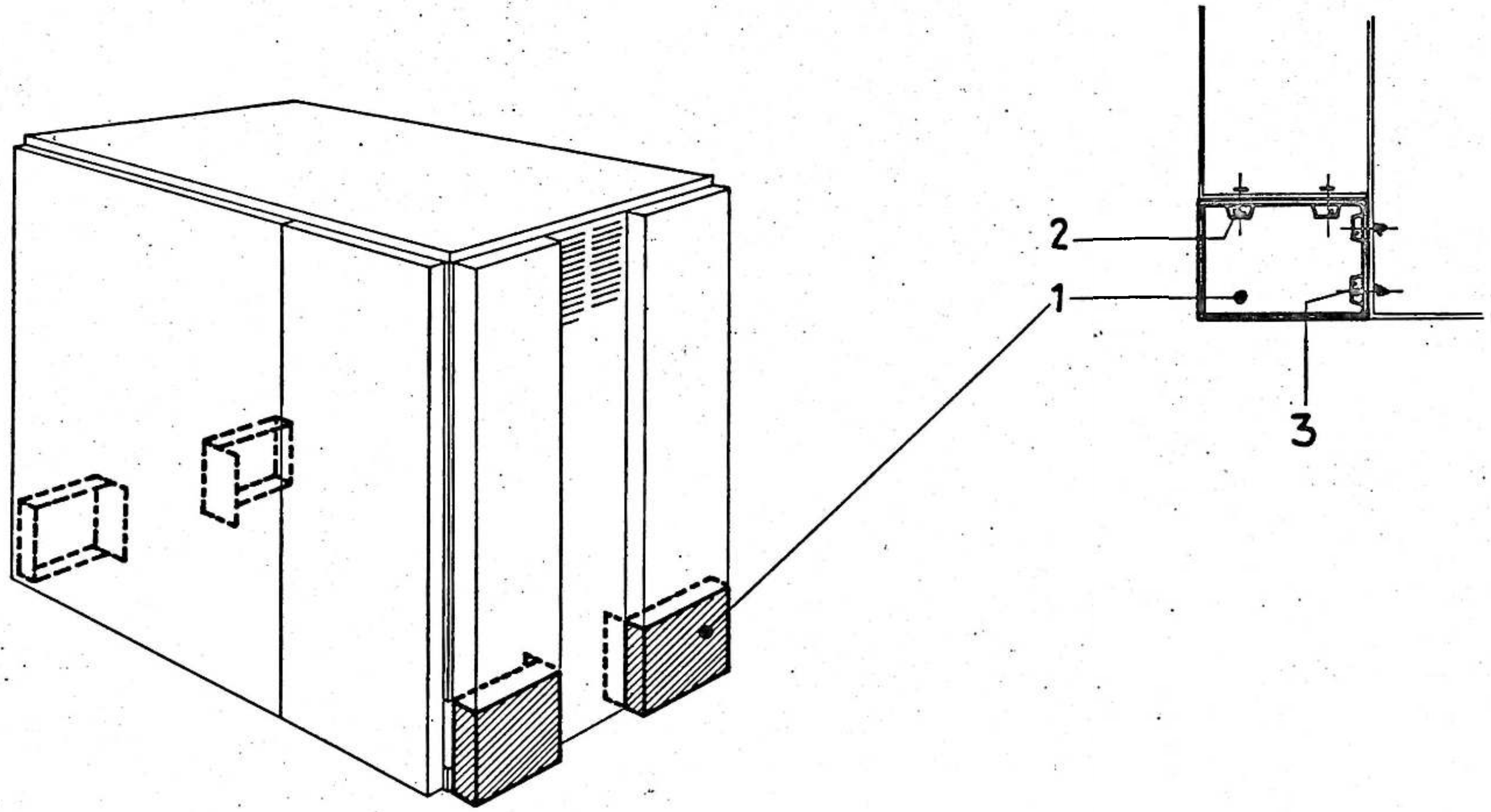
Cod. 3896104 Q
66.10.30

78B103796

REVISIONI					
REV	ORD. APPL.	DATA			FIRMA
		A	M	G	
A	CO M100826	71	03	16	Alberti P.

VERSIONE DOPPIO PAVIMENTO

DOUBLE FLOOR VERSION



ITEM NUMBERS SHOWN
APPLY TO MOD KIT
78X103795 G2

NOTES

PARTI NUMERATE
SECONDO LISTA N°
78X103795 G2

NOTE

SALVO INDICAZIONE CONTRARIA DIMENSIONI: MILLIMETRI / INCH TOLLERANZE DIMENS. E DI FORMA VEDI: PROIEZIONE	MAT.	**Honeywell** Honeywell Information Systems Italia
	TT.	DESCRIZIONE VERSIONE DOPPIO PAVIMENTO INSTALLAZ. PARTI
	FIN.	
SCALA / COD.	DISEGNATO 70 DIC. 30 Cecchini Sebastiano	DISEGNO 78B103796 / PAG 1/1 / REV A
	APPROVATO	
	DISTR.	

S. T.

CODICI			
G2	0814018P	G6	
G3		G7	
G4		G8	

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Honeywell Information Systems Italia

PL 78X103795 PAG. 1/2 REV.

*	POS. NO	C D	NUMERO DI IDENTIFICAZIONE	DESCRIZIONE DELLA PARTE		G1	G2	G3	G4	G5	G6	G7	G8	U M
	1	0	08052 039	TAPPO CAN. CAVI	0817208W	2	4							EA
	2	1	6311242 W	VITE TC M4x8	6311242W	4	8							EA
	3	1	0005343 D	VITE AUT. ϕ4.2x9.5	0005343D	4	8							EA
	4	0	78A100196 G1	COPERCHIO STRETTO	0674529T	2								EA
	5	0	08544 384	ELEM. DI COLLEG.	0674185Y	1								EA
	6	0	08544 386	ELEM. DI COLLEG.	0674187G	1								EA
	7	0	08054 033	PIASTRINA	0836464Z	2								EA
	8	0	78C100200 G1	PEDANA SPECIALE	0674533A	2								EA
	9	1	6313725 B	VITE TS M5x20	6313725B	8								EA
	10	1	6312743 Q	VITE TS M4x8	6312743Q	2								EA
	11	0	08544350	COPERTURA LAT.	0674390T	1								EA
	12	0	08041829	PEDANA	0835988K	3								EA
	13	0	08043823	COPERCHIO IMB. TEST.	0835823M	2								EA
	14	1	6312748 E	VITE TS M4x20	6312748E	2								EA
	15	1	6313204 F	VITE TC C.E M10x30	6313204F	2								EA
	16	1	6313169U	VITE TC C.E. M8x30	6313169U	4								EA

S.T.

CD - CODICE DI DISEGNO
0 - DISEGNO ISG
1 - PARTE ACQUISTATA A CATALOGO
2 - RICHIAMO DI PIU' ALTERNATIVE
3 - PARTE A CATALOGO DA MODIFICARE
4 - PARTE ISG DA MODIFICARE
5 - PARTE DA SELEZIONARE

UM - UNITA' DI MISURA
EA
~~N~~ - NUMERO
IN - INCH
G - GRAMMO
CM - CENTIMETRO

* ULTIME POSIZIONI MODIFICATE

DESCRIZIONE
KIT PARTI
DSS. 157

PL 78X103795 PAG. 1/2 REV. A

Cod. 3898111 G

PER LE MODIFICHE VEDI FOGLIO REVISIONE

88.10.30

Honeywell
Honeywell Information Systems Italia

PL 78X103795 PAG. 2F REV.

*	POS. NO	C D	NUMERO DI IDENTIFICAZIONE	DESCRIZIONE DELLA PARTE		G1	G2	G3	G4	G5	G6	G7	G8	U M
	17	1	6331108Y	RONDELLA 8.4	6331108Y	8								EA
	18	1	6321108X	DADO M8	6321108X	4								EA
	19	1	6313206 P	VITE TC C.E. M10x40	6313206P	6								EA
	20	1	6331110 N	ROND. PIANA 10,5	6331110N	16								EA
	21	1	6332110 S	ROND. EL. 10.5	6332110S	8								EA
	22	1	6321110 M	DADO M10	6321110M	8								EA
	23	0	08041820	COPERCHIO PIATTO	0835821D	1								EA
	24	0	788103794	INSTALL. PARTI		X								
	25	0	78B103796	INSTALL. PARTI			X							

S.T.

CD - CODICE DI DISEGNO
0 - DISEGNO ISG
1 - PARTE ACQUISTATA A CATALOGO
2 - RICHIAMO DI PIU' ALTERNATIVE
3 - PARTE A CATALOGO DA MODIFICARE
4 - PARTE ISG DA MODIFICARE
5 - PARTE DA SELEZIONARE

UM - UNITA' DI MISURA
EA
~~N~~ - NUMERO
IN - INCH
G - GRAMMO
CM - CENTIMETRO

* ULTIME POSIZIONI MODIFICATE

DESCRIZIONE
KIT PARTI

PL 78X103795 PAG. 2F REV. A

78B103858

REVISIONI					
REV	ORD. APPL.	DATA A	M	G	FIRMA
A	CO M100 828	71	03	16	Alberti P.

	RIF. REF.	TIPO TYPE	△2			MARCATURA E COLLEGAMENTO CAVI CABLE CONNECTION AND MARKING △3		FUNZ. FUNCT.	NOTE NOTES
△1			G1	G2	G3	LATO INT. ALL' U.F. SIDE INT. TO PH. UNIT	LATO EST. ALL' U.F. SIDE EST. TO PH.UNIT		
	C1	AL 171	1			I CLUSTER AC-IN	DSC 157 ALI 260 TL1-R	AC.	
							S		
							T		
							GR		
	C2	NS 158	2			I CLUSTER J4	DSC 157 GUD 040 Y11	LOG	
	C3	NS 132	3			I CLUSTER J1	DSC157 VAR 586 Y1	LOG	
	C4	NS 132	3			I CLUSTER J2	DSC 157 VAR586 Y2	LOG	
	C5	NS 132	3			I CLUSTER J3	DSC 157 VAR 586 Y3	LOG	
	TP5		4			CONN. TAPPO		LOG	△12
	C6	NS 132		7		II CLUSTER J1	DSC 157 VAR586 Y4	LOG	
	C7	NS 132		7		II CLUSTER J2	DSC 157 VAR586 Y5	LOG	
	C8	NS 132		7		II CLUSTER J3	DSC 157 VAR586 Y6	LOG	
	C9	AL 177		5		II CLUSTER AC-IN	I CLUSTER AC-OUT	A.C.	
	C10	NS 158		6		II CLUSTER J4	I CLUSTER J5	LOG	
	C11	NS 132			8	III CLUSTER J1	DSC 157 VAR586 Y7	LOG	
	C12	NS 132			8	III CLUSTER J2	DSC 157 VAR586 Y8	LOG	
	C13	NS 132			8	III CLUSTER J3	DSC 157 VAR 586 Y9	LOG	
	C14	AL 177			5	III CLUSTER AC-IN	II CLUSTER AC-OUT	A.C.	
	C15	NS 158			6	III CLUSTER J4	II CLUSTER J5	LOG	

FOR THE CABLES ASSEMBLY SIDE REF. TO DRAW No. 78C103857

12. TERMINATOR TP5 MUST BE ASSEMBLED ON JOS CONNECTOR OF THE LAST CLUSTER.

11 - YELLOW-GREEN
10 - WHITE
9 - GREEN
8 - BROWN
7 - BLUE
6 - RED
5 - BLACK
4 - YELLOW

△3 - SEE LABELLING INSTRUCTION DRAWING No 09874 010

△2 - ITEM NUMBERS SHOWN APPLY TO DRAWING No 78X103856

△1-X - PARTS ASSEMBLED WHEN DELIVERED

NOTES

PER IL MONTAGGIO CAVI VEDI DIS. 78C103857

12. IL CONNETTORE TAPPO TP5 VA MONTATO IN POSIZIONE JOS DELL'ULTIMO CLUSTER

11 - GIALLO-VERDE
10 - BIANCO
9 - VERDE
8 - MARRONE
7 - BLU
6 - ROSSO
5 - NERO
4 - GIALLO

△3 - VEDERE ISTRUZ. MARCATURA DIS. No 09874 010

△2 - PARTI NUMERATE SECONDO LISTA DIS 78X103856

△1-X - PARTI MONTATE ALLA SPEDIZIONE

NOTE

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Honeywell Information Systems Italia

SALVO INDICAZIONE CONTRARIA
DIMENSIONI: MILLIMETRI / INCH
TOLLERANZE DIMENS. E DI FORMA VEDI:
PROIEZIONE
SCALA
COD.

MAT.
TT.
FIN.
DISEGNATO 41-GEN22 Moroni
APPROVATO
DISTR.

DESCRIZIONE
MARC. E COLL. CAVI DSU167

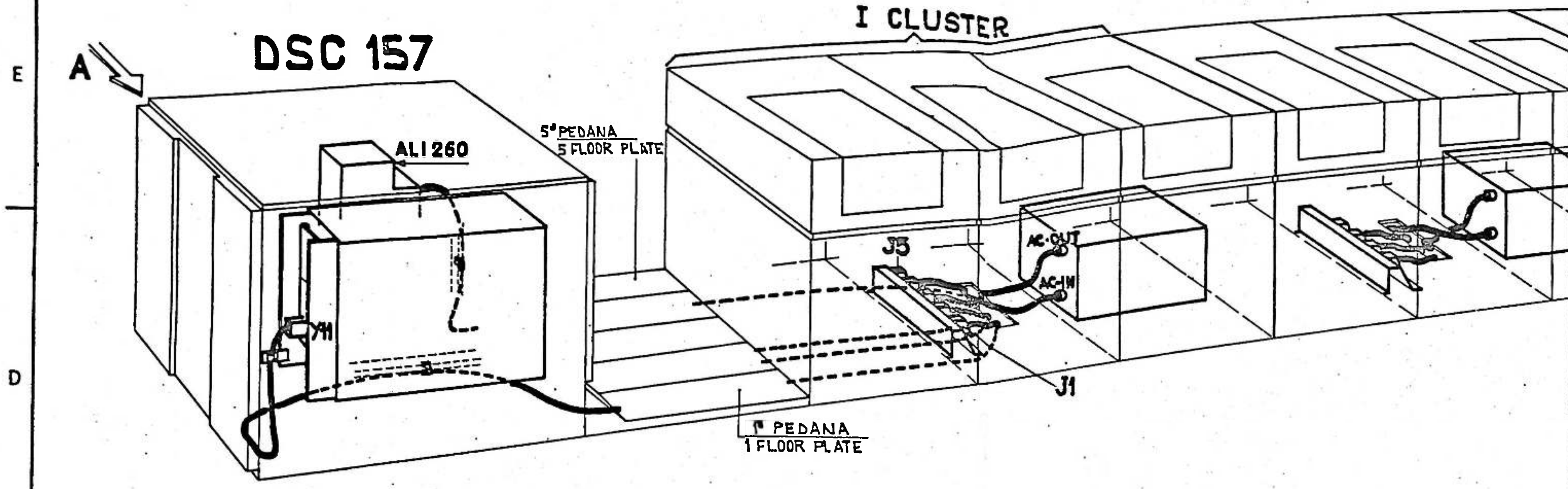
DISEGNO
78B103858

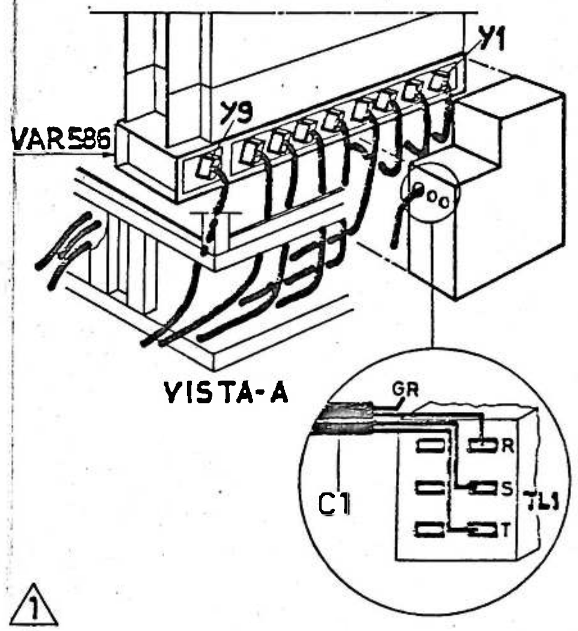
PAG 1/1
REV A

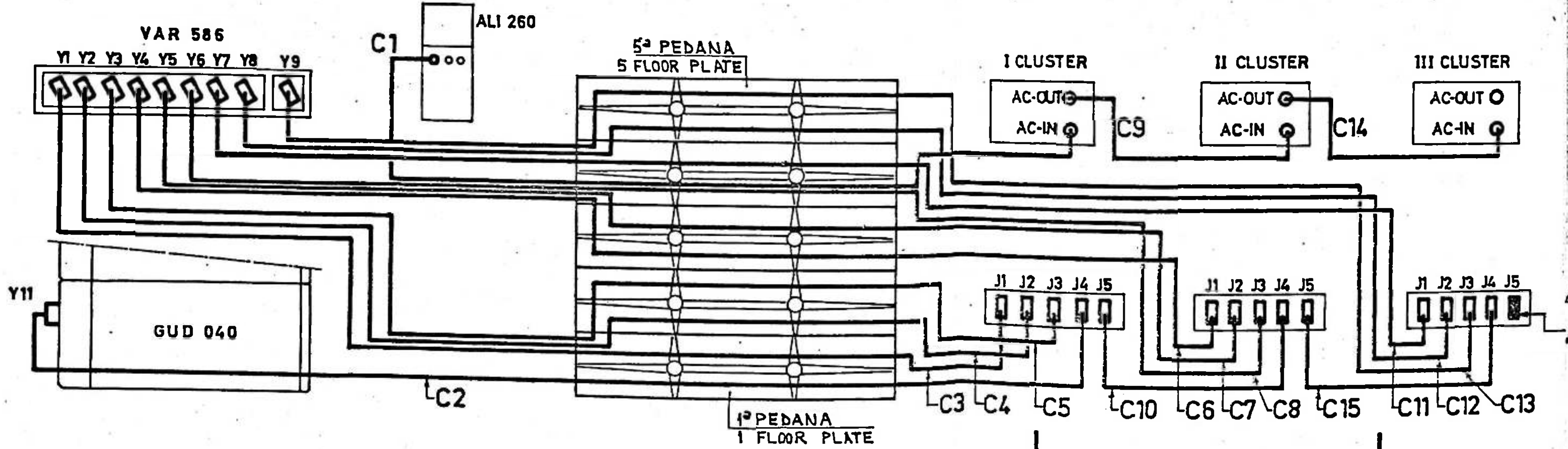
S.T.

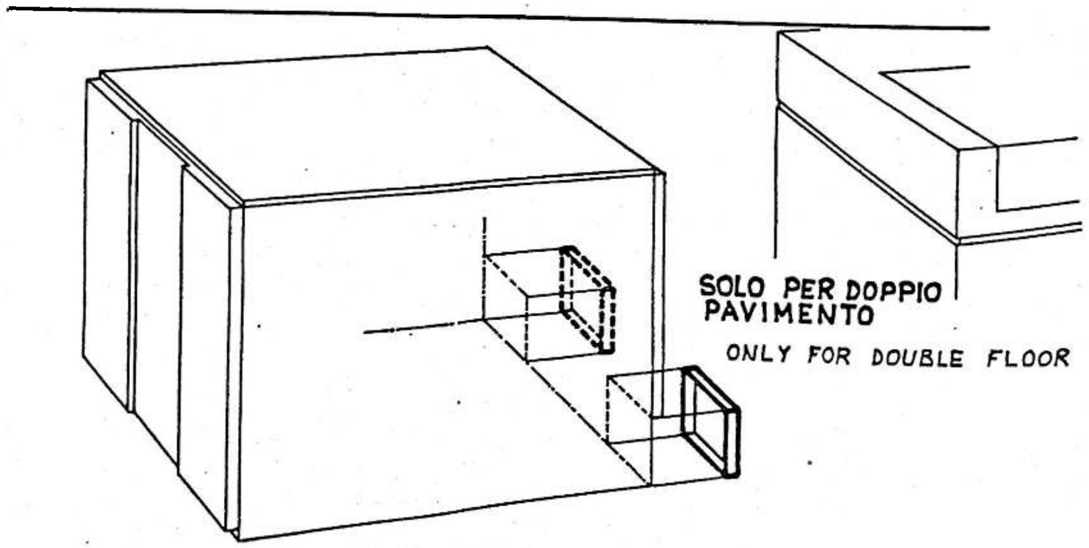
REVISIONI					
REV	ORD. APPL.	DATA			FIRMA
		A	M	G	
A	CO M100828	71	03	16	Alberti Paolo

POS.	CAVO-CABLE
1	C1
2	C2
3	C3-C4-C5
5	C9-C14
6	C10-C15
7	C6-C7-C8
8	C11-C12-C13








SOLO PER DOPPIO PAVIMENTO

ONLY FOR DOUBLE FLOOR

S.T.

NOTES:

△1_ TERMINATOR POS. 4 MUST BE ASSEMBLED ON THE LAST CLUSTER

NUMERATED PARTS ACCORDING TO LIST 78X103856

NOTE:

△1_ IL TAPPO A POS. 4 VA MONTATO SU L'ULTIMA CLUSTER

PARTI NUMERATE SECONDO LISTA 78X103856

SALVO INDICAZIONE CONTRARIA DIMENSIONI: MILLIMETRI / INCH TOLLERANZE DIMENS. E DI FORMA VEDI: PROIEZIONE	MAT.	**Honeywell** Honeywell Information Systems Italia
	TT.	DESCRIZIONE INSTALLAZIONE CAVI
	FIN.	
SCALA	COD.	DISEGNATO 71 GEN 22 Moroni	DISEGNO 78C103857 · PAG 1/1 · REV A
		APPROVATO	
		DISTR.	

Cod. 3999106Y

681030

CODICE			
G1	0643465C	G5	
G2	0643466Q	G6	
G3	0643467L	G7	
G4		G8	

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Honeywell Information Systems Italia

PL 78X103856 — PAG. 1/1 — REV.

*	POS. NO	CD	NUMERO DI IDENTIFICAZIONE	DESCRIZIONE DELLA PARTE		GRUPPI E QUANTITA' G1	G2	G3	G4	G5	G6	G7	G8	UM
	1	0	78A104207 G2	CAVO AL 171	0640880U	1								EA
	2	0	78A103290 G2	CAVO NS 158	0640213Z	1								EA
	3	0	78A104201 G1	CAVO NS 132	0640161L	3								EA
	4	0	78B103338G3	CONNETTORE TAPPO	0818164A	1								EA
	5	0	78A104211 G3	CAVO AL 177	0640897F		1	1						EA
	6	0	78A103290 G1	CAVO NS 158	0640212V		1	1						EA
	7	0	78A104201 G2	CAVO NS 132	0640162Y		3							EA
	8	0	78A104201 G4	CAVO NS 132	0640164R			3						EA
	9	0	78103858	MARC. E COLL. CAVI		X	X	X						
	10	0	78C103857	INSTALL. CAVI		X	X	X						

S. T.

CD - CODICE DI DISEGNO
0 - DISEGNO ISG
1 - PARTE ACQUISTATA A CATALOGO
2 - RICHIAMO DI PIU' ALTERNATIVE
3 - PARTE A CATALOGO DA MODIFICARE
4 - PARTE ISG DA MODIFICARE
5 - PARTE DA SELEZIONARE

U.M. - UNITA' DI MISURA
EA
Nº - NUMERO
IN - INCH
G - GRAMMO
CM - CENTIMETRO

✱ ULTIME POSIZIONI MODIFICATE

DESCRIZIONE
KIT CAVI DSU 167
PL 78X103856 — PAG. 1/1 — REV. A

Cod. 3898111G

PER LE MODIFICHE VEDI FOGLIO REVISIONE

68.10.30

B78106808

REVISIONI					
REV	ORD. APPL.	DATA A	M	G	FIRMA

①	RIF. REF.	TIPO TYPE	② 001	002	003	MARCATURA E COLLEGAMENTO CAVI CABLE CONNECTION AND MARKING ③ LATO INT ALL' U.F. SIDE INT. TO PH. UNIT	LATO EST. ALL' U.F. SIDE EST. TO PH.UNIT	FUNZ. FUNCT.	NOTE NOTES
	C1	AL171	1			I DSU AC-IN	DSC157 ALI260 TL1-R	A.C.	
							S		
							T		
							G		
	C2	NS158	2			I DSU J100	DSC157 GUD040 Y11	LOG.	
	C3	NS132	3			I DSU J102	DSC157 VAR586 Y1	LOG.	
	TP5		4			CONN. TAPPO			4
	C4	AL177		6		II DSU AC-IN	I DSU AC-OUT	A.C.	
	C5	NS158		7		II DSU J100	I DSU J101	LOG.	
	C6	NS132		8		II DSU J102	DSC 157 VAR586 Y2	LOG	
	C7	AL177			6	III DSU AC-IN	II DSU AC-OUT	A.C.	
	C8	NS158			7	III DSU J100	II DSU J101	LOG.	
	C9	NS132			10	III DSU J102	DSC 157 VAR586 Y3	LOG	

FOR THE CABLES ASSEMBL'
SIDE REF. TO DRAW No. C78106809
△2. item numbers shown apply
to draw. no. X78106807 where:
G1 = Cables Kit for I DSU
G2 = Cables Kit for II DSU
G3 = Cables Kit for III DSU
△4. Terminator TP5 must be
assembled on J 101 connector
of the last unit

△3 - SEE LABELLING INSTRUCTION
DRAWING No 09874 010

~~△2 ITEM NUMBERS SHOWN APPLY TO~~
~~DRAWING N.~~

△1-X - PARTS ASSEMBLED
WHEN DELIVERED

NOTES

PER IL MONTAGGIO CAVI
VEDI DIS. C78106809
△2 - Parti numerate secondo
P.L. X78106807 dove:
G1 = Kit cavi I DSU 157 D
G2 = Kit cavi II DSU 157 D
G3 = Kit cavi III DSU 157 D
△4 Il connettore tappo TP5
va montato in posizione J101
dell'ultima DSU del sottosistema

△3 - VEDERE ISTRUZ. MARCATURA
DIS. No 09874 010

~~△2 - PARTI NUMERATE SECONDO~~
~~LISTA DIS.~~

△1-X - PARTI MONTATE ALLA
SPEDIZIONE

NOTE

SALVO INDICAZIONE CONTRARIA
DIMENSIONI: MILLIMETRI / INCH
TOLLERANZE DIMENS. E DI FORMA VEDI:
PROIEZIONE
SCALA
COD.
MAT.
TT.
FIN.
DISEGNATO
APPROVATO
DISTR.

Honeywell
Honeywell Information Systems Italia

DESCRIZIONE
MARC. E COLL. CAVI DSU 157 D
DISEGNO
B78106808
PAG 1/3
REV B

B78106808

REVISIONI

REV	ORD. APPL.	DATA A	DATA M	DATA G	FIRMA

MARCATURA E COLLEGAMENTO CAVI
CABLE CONNECTION AND MARKING △3

△1	RIF. REF.	TIPO TYPE	△2 004	005	006	LATO INT. SIDE INT.	ALL' U.F. TO PH. UNIT	LATO EST. SIDE EST.	ALL' U.F. TO PH.UNIT	FUNZ. FUNCT.	NOTE NOTES
	C10	AL177	6			IV DSU	AC-IN	III DSU	AC-OUT	A.C.	
	C11	NS158	7			IV DSU	J100	III DSU	J101	LOG.	
	C12	NS132	10			IV DSU	J102	DSC157 VAR586	Y4	LOG.	
	C13	AL177		6		V DSU	AC-IN	IV DSU	AC-OUT	A.C.	
	C14	NS158		7		V DSU	J100	IV DSU	J101	LOG.	
	C15	NS132		13		V DSU	J102	DSC157 VAR586	Y5	LOG.	
	C16	AL177			6	VI DSU	AC-IN	V DSU	AC-OUT	A.C.	
	C17	NS158			7	VI DSU	J100	V DSU	J101	LOG.	
	C18	NS132			15	VI DSU	J102	DSC157 VAR586	Y6	LOG.	

FOR THE CABLES ASSEMBLY
SIDE REF. TO DRAW No. C78106809

△2. item numbers shown apply
to draw. no. X78106807 where:
G4 = cables Kit for IV DSU
G5 = cables Kit for V DSU
G6 = cables Kit for VI DSU

△3 - SEE LABELLING INSTRUCTION
DRAWING No 09874 010

~~△2 - ITEM NUMBERS SHOWN APPLY TO~~
~~DRAWING No~~

△1-X - PARTS ASSEMBLED
WHEN DELIVERED

NOTES

PER IL MONTAGGIO CAVI
VEDI DIS. C78106809

△2. Parti numerate secondo
P.L. X78106807 dove:
G4 = Kit cavi IV DSU157D
G5 = Kit cavi V DSU157D
G6 = Kit cavi VI DSU157D

△3 - VEDERE ISTRUZ. MARCATURA
DIS. No 09874 010

~~△2 - PARTI NUMERATE SECONDO~~
~~LISTA DIS.~~

△1-X - PARTI MONTATE ALLA
SPEDIZIONE

NOTE

SALVO INDICAZIONE CONTRARIA
DIMENSIONI: MILLIMETRI / INCH
TOLLERANZE DIMENS. E DI FORMA VEDI:
PROIEZIONE
SCALA
COD.
MAT.
TT.
FIN.
DISEGNATO
APPROVATO
DISTR.

Honeywell
Honeywell Information Systems Italia

DESCRIZIONE
MARC. E COLL. CAVI DSU157D

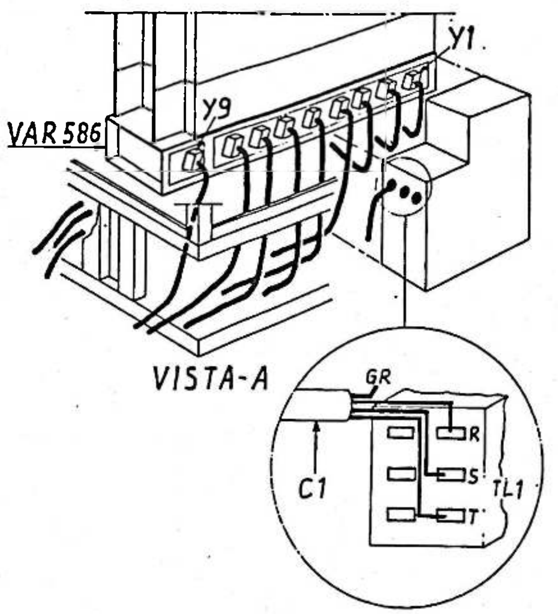
DISEGNO
B78106808

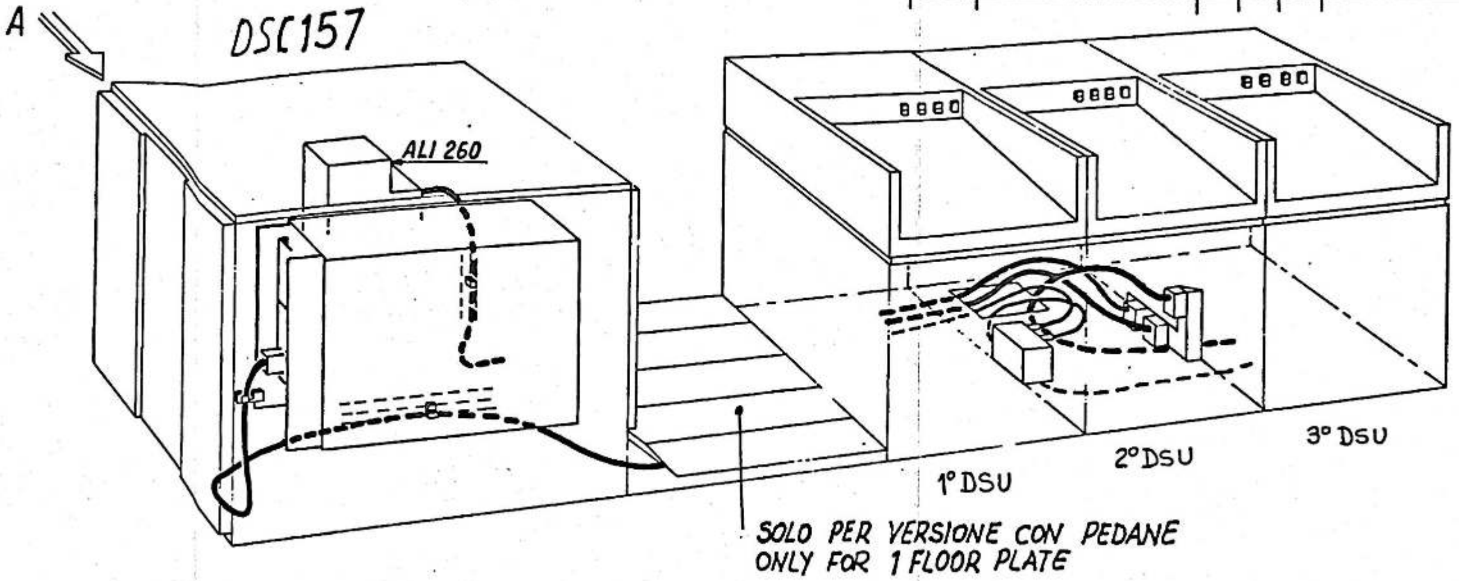
PAG
2

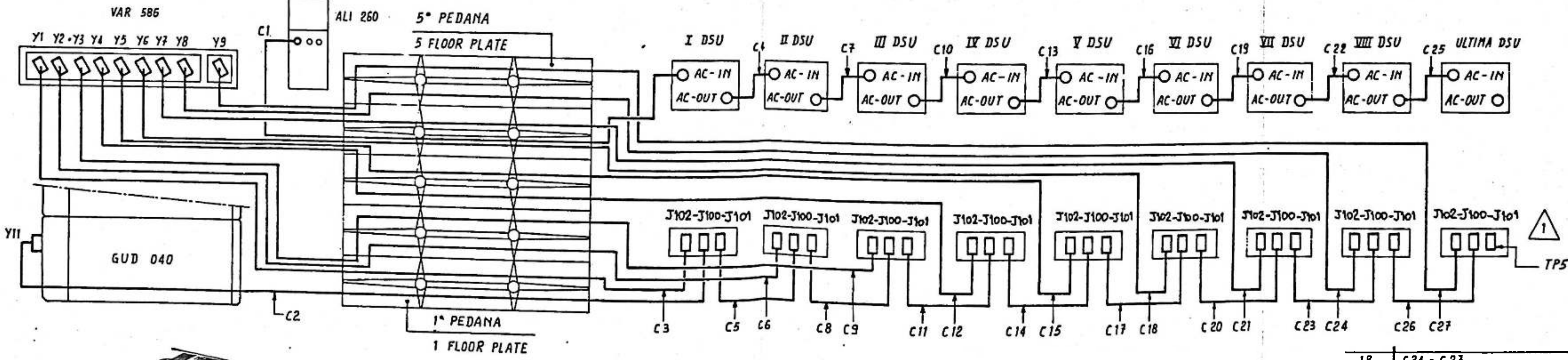
REV
B

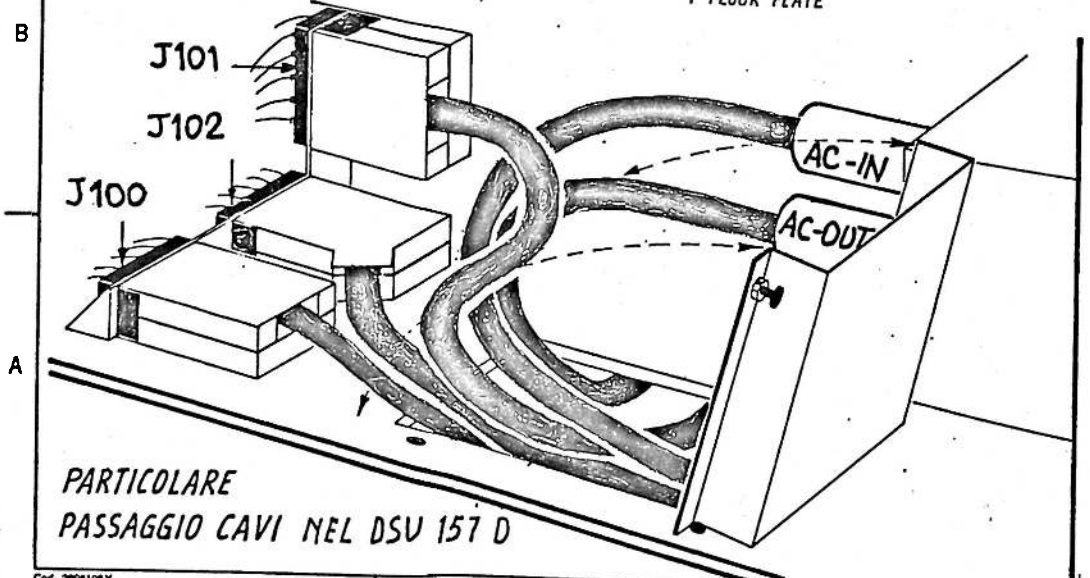
Mod. 1133

REVISIONI					
REV	ORD. APPL.	DATA			FIRMA
		A	M	G	
A	C.O. M101346	72	07	06	·
B	C.O. M101368	72	09	08	Rinaldi









PARTICOLARE
PASSAGGIO CAVI NEL DSU 157 D

NOTES :

△ 1 - TERMINATOR PT5 POS.4 MUST BE ASSEMBLED ON THE LAST UNIT

NUMERATED PARTS ACCORDING TO LIST X78106807

NOTE :

△ 1 - IL TAPPO TP5 POS.4 VA MONTATO SULL' ULTIMA DSU

PARTI NUMERATE SECONDO LISTA X78106807

POS.	CAVO-CABLE
18	C24 - C27
15	C18 - C21
13	C15
10	C9 - C12
8	C6
7	C5 - C8 - C11 - C14 - C17 - C20 - C23 - C26
6	C4 - C7 - C10 - C13 - C16 - C19 - C22 - C25
4	TP5
3	C3
2	C2
1	C1

SALVO INDICAZIONE CONTRARIA
DIMENSIONI: MILLIMETRI / INCH
TOLLERANZE DIMENS. E DI FORMA VEDI:
PROIEZIONE
SCALA
COD.
27/6/1972
MAT.
TT.
FIN.
DISEGNATO Giusto Rolando
APPROVATO
DISTR.

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Honeywell Information Systems Italia

DESCRIZIONE
INSTALLAZIONE CAVI

DISEGNO
C 78106809

PAG 1/1
REV B

C 78106809

Cod. 3896108Y

HIS ITALIA CODICE			
001	0811	005	0811105 N
002	0811102 Z	006	0811106 S
003	0811103V	007	0811107 W
004	0811104J	008	0811108 K

X78106807 1/3

*	ITEM NO.	P. C.	IDENTIFICATION NUMBER	S. C.	DRAWING TITLE	001	002	003	004	005	006	007	008	U. M.
						ASSEMBLY / QUANTITY								
	1		78A104207_G1		CAVO AL 171 0640879N	1								EA
	2		78A103290_G1		CAVO NS 158 0640212V	1								EA
	3		78A104201-G6		CAVO NS132 0640165M	1								EA
	4		78B103338-G3		CONN. TAPPO 0818164A	1								EA
	5		60205060 -010		PLUG NOME UNITÀ "0"	1								EA
	6		78A104211-G1		CAVO AL177 0640896B		1	1	1	1	1	1	1	EA
	7		78A103290-G3		CAVO NS 158 0640214N		1	1	1	1	1	1	1	EA
	8		78A104201-G1		CAVO NS 132 0640161L		1							EA
	9		60205060- 001		PLUG NOME UNITÀ "1"		1							EA
	10		78A104201-G7		CAVO NS132 0640166Z			1	1					EA
	11		60205060 -002		PLUG NOME UNITÀ "2"			1						EA
	12		60205060 _003		PLUG NOME UNITÀ "3"				1					EA
	13		78A104201-G2		CAVO NS132 0640162Y					1				EA
	14		60205060 - 004		PLUG NOME UNITÀ "4"					1				EA
	15		78A104201-G3		CAVO NS 132 0640163Y						1	1		EA
	16		60205060 -005		PLUG NOME UNITÀ "5"						1			EA

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Loc. PREGNANA MILANESE, ITALIA

U.M.-UNIT OF MEASURE
EA - EACH
CM - CENTIMETER
G - GRAMS
IN - INCHES
OZ - OUNCE

* ITEMS REVISED SINCE PREVIOUS ISSUE

TITLE
KIT CAVI DSU157D
SIZE X
P.L. NO. 78106807
SHEET 1/3
REV. B

DOES A DOCUMENT REVISION STATUS SHEET EXIST? ☐

HIS ITALIA CODICE			
001		005	
002		006	
003		007	0811107 W
004		008	0811108 K

X78106807 2

*	ITEM NO.	P. C.	IDENTIFICATION NUMBER	S. C.	DRAWING TITLE	001	002	003	004	005	006	007	008	U. M.
						ASSEMBLY / QUANTITY								
	17		60205060 -006		PLUG NOME UNITÀ "6"							1		EA
	18		78A104201_G4		CAVO NS 132 0640164R								1	EA
	19		60205060 - 007		PLUG NOME UNITA "7"								1	EA

Honeywell
Honeywell Information Systems Italia
Loc. PREGNANA MILANESE, ITALIA

U.M.-UNIT OF MEASURE
EA - EACH
CM - CENTIMETER
G - GRAMS
IN - INCHES
OZ - OUNCE

* ITEMS REVISED SINCE PREVIOUS ISSUE

TITLE
KIT CAVI DSU157D
SIZE X
P.L. NO. 78106807
SHEET 2
REV. A

DOES A DOCUMENT REVISION STATUS SHEET EXIST? ☐

HIS ITALIA CODICE			
009	0811109 P	013	
010		014	
011		015	
012		016	

X 78106 807	3/F	

*	ITEM NO.	P. C.	IDENTIFICATION NUMBER	S. C.	DRAWING TITLE	ASSEMBLY / QUANTITY								U. M.
						009	010	011	012	013	014	015	016	
	6		78A104211_G1		CAVO AL 177 0640896B	1								EA
	7		78A103290_G3		CAVO NS158 0640214 N	1								EA
	18		78A104201_G4		CAVO NS 132 0640164R	1								EA
	20		60205060_ 009		PLUG NOME UNITA' "S"	1								EA

Honeywell

Honeywell Information Systems Italia

Loc. PREGNANA MILANESE, ITALIA

U.M.-UNIT OF MEASURE

EA – EACH	IN – INCHES
CM – CENTIMETER	OZ – OUNCE
G – GRAMS	

* ITEMS REVISED SINCE PREVIOUS ISSUE

TITLE
KIT CAVI DSU 157 D

SIZE	P.L. NO.	SHEET	REV.
X	78106807	3/F	B

DOES A DOCUMENT REVISION STATUS SHEET EXIST? ☐

B78106811

△1	RIF. REF.	TIPO TYPE	△2 001	△2 002	MARCATURA E COLLEGAMENTO CAVI / CABLE CONNECTION AND MARKING △3 LATO INT. ALL' U.F. SIDE INT. TO PH. UNIT	MARCATURA E COLLEGAMENTO CAVI / CABLE CONNECTION AND MARKING △3 LATO EST. ALL' U.F. SIDE EST. TO PH.UNIT	FUNZ. FUNCT.	NOTE NOTES
		AL 177	1		IV DSU AC-IN	I CLUSTER AC-OUT	AC.	4
		NS 158	2		IV DSU J4	I CLUSTER J5	LOG.	4
		NS 132	3		IV DSU J1	DSC 157 VAR586 Y4	LOG.	4
		AL 177		5	VII DSU AC-IN	II CLUSTER AC-OUT	AC.	4
		NS 158		6	VII DSU J4	II CLUSTER J5	LOG.	4
		NS 132		7	VII DSU J1	DSC157 VAR586 Y7	LOG.	4

REVISIONI

REV	ORD. APPL.	DATA A	DATA M	DATA G	FIRMA

FOR THE CABLES ASSEMBLY SIDE REF. TO DRAW No. C78106809 and 78C103857

△2. item numbers shown apply to draw. n.o X 78106810 where:
G1 = cables Kit for DSU157D (IV) subsequent at I CLUSTER DSU167
G2 = cables Kit for DSU157D (VII) subsequent at II CLUSTER DSU 167

△4. for cables Kit corresponding to DSU157D subsequents at IV or VII see draw. B78106808

△3 - SEE LABELLING INSTRUCTION DRAWING No 09874 010

~~△2 - ITEM NUMBERS SHOWN APPLY TO DRAWING No~~

△1-X - PARTS ASSEMBLED WHEN DELIVERED

NOTES

PER IL MONTAGGIO CAVI VEDI DIS. C78106809 e 78C103857

△2. Parti numerate secondo P.L. X78106810 dove:
G1 = Kit cavi per DSU 157D (IV) successiva a I CLUSTER DSU167.
G2 = Kit cavi per DSU157D (VII) successiva a II CLUSTER DSU 167

△4 Per Kit cavi relativi a DSU157D successive alla IV o alla VII consultare dis. B78106808

△3 - VEDERE ISTRUZ. MARCATURA DIS. No 09874 010

~~△2 - PARTI NUMERATE SECONDO LISTA DIS.~~

△1-X - PARTI MONTATE ALLA SPEDIZIONE

NOTE

SALVO INDICAZIONE CONTRARIA
DIMENSIONI: MILLIMETRI / INCH
TOLLERANZE DIMENS. E DI FORMA VEDI:
PROIEZIONE
SCALA
COD.

MAT.
TT.
FIN.
DISEGNATO
APPROVATO
DISTR.

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DESCRIZIONE AMPLIAMENTO (DSU167 + DSU157D)
MARC. E COLL. CAVI UNITÀ MISTE

DISEGNO B78106811
PAG 1/1
REV. A

Mod. 1153

HIS ITALIA CODICE			
001	4010003R	005	
002	4010004E	006	
003		007	
004		008	

X78106810	1/1	

*	ITEM NO.	P. C.	IDENTIFICATION NUMBER	S. C.	DRAWING TITLE	ASSEMBLY / QUANTITY								U. M.
						001	002	003	004	005	006	007	008	
	1		78A104211-G3		CAVO AL 177	1								EA
	2		78A103290-G1		CAVO NS 158	1								EA
	3		78A104201-G7		CAVO NS 132	1								EA
	4		60205060- 003		PLUG NOME UNITÀ "3"	1								EA
	5		78A104211-G3		CAVO AL 177		1							EA
	6		78A103290-G1		CAVO NS 158		1							EA
	7		78A104201-G3		CAVO NS 132		1							EA
	8		60205060- 006		PLUG NOME UNITÀ "6"		1							EA

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Loc. PREGNANA MILANESE, ITALIA

U.M. - UNIT OF MEASURE

EA - EACH
CM - CENTIMETER
G - GRAMS
IN - INCHES
OZ - OUNCE

* ITEMS REVISED SINCE PREVIOUS ISSUE

TITLE AMPLIAMENTO DSU 167 + DSU 157D
KIT CAVI UNITÀ MISTE

SIZE	P.L. NO.	SHEET	REV.
X	78106810	1/1	A

DOES A DOCUMENT REVISION STATUS SHEET EXIST ? ☐

MAINTENANCE

Honeywell

Honeywell Information Systems Italia

DSC 161/162/150/157

DISC STORAGE CONTROLLERS

Maintenance

FIFTH EDITION

A Field Engineering
publication

4.813.4.001.4/A

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Honeywell Information Systems Italia

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N.B. Remove pages identified with crossed numbers

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1. OPERATOR TASKS

Note

No operator level routine has been foreseen.

2. MAINTENANCE CHECKS

ROUTINE : **2.1**

NAME : ALI 130 (DSC 161-162-150) and ALI 130B (DSC 157) OUTPUT VOLTAGE AND RIPPLE

DURATION : 0.10 hr.
PREREQUISITES : The Power Supply must function correctly.

1 - NEEDED MATERIAL

- Multimeter, class 1.5	P.N. 5282624 A
- Multimeter prods	" 5282628 B
- Oscilloscope Tektronix 422	

2 - PURPOSE

- Check that the output voltage is maintained within the limits given in the general features (PDS).
- Check that the ripple, on the output voltages, is maintained within the limits given in the general features (PDS).

3 - PRELIMINARY CHECKS

- Ascertain that the Power Supply is set to the "External Load" position.
- Zero the multimeter.
- Check for correct setting of the scope's vertical amplifier.

4 - PROCEDURE

1) - Gain access to the Power Supply (box side).

2) - Check with the meter that the box socket voltages, result within the hereby given limits:

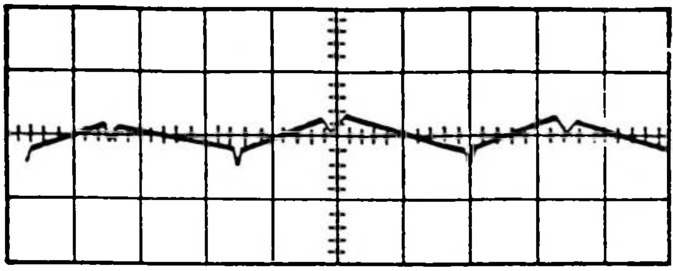
BOX	NOMINAL VOLTAGE	SPEC. LIMITS	MAX RIPPLE
± 3	-3 V	-2.88V to -3.12V	15 mV
± 3	+3 V	+2.88V to +3.12V	15 mV
+ 5	+5.2 V	+4.95V to +5.45V	50 mV
+ 6*	+6 V	+5.75V to +6.25V	50 mV
- 36	-36 V	-34.55V to -37.45V	50 mV

* Only for ALI 130 (DSC161/162/150)

3) - Should one or more voltages result out of the above limits, implement routine 4.1 (Output voltage adjustment); otherwise proceed with step 4.

4) - Connect up the scope ground and a channel to the appropriate voltage box sockets.

Ripple must result within the limits given in the above table and resemble the form shown in fig. 2.1.



Scale

0.5 µsec/cm - 50 mV/cm

Sync. on INT. - AUTO -

AC

Fig. 2.1. - Ripple Waveform

5) - Should the monitored waveform result completely different from the illustration in fig. 2.1, implement routine 4.1.

6) - With all the load switch jumper straps set to the "External Load" position, place the multimeter prods (remember to set the multimeter on the correct DC scale) across the last subsystem unit ground and sockets "+ 3V", "- 3V", "- 36V", "+ 6V" (for DSU 160 B/C and DSU 110) or "+ 5V" (for DSU 167 and DSU 157 D/E).

Note

Depending upon the unit under test, the various test points or sockets can be found on:

- the maintenance panel (front side of unit) for DSU 160B
- the rear side of the unit for DSU 160C.
- the front side of the unit (ATA 100) for DSU 110
- the rear side of the electronic panel (module A) for DSU 167.

For the DSU 157 D/E units, voltage must be measured on the A5H board pin 44 (+3V), pin 25 (-3V), pin 29 (+5V), pin 26 (-36V).

7) - Check that the voltage value results within the spec. limits given in the table at step 2.

8) - Set the subsystem to its normal functioning state.

5 - FINAL CHECKS

- None.

ROUTINE : 2.2

NAME : CPU +20 V RIPPLE

DURATION : 0.1 hr
PREREQUISITES : None

1 - NEEDED MATERIAL

- Oscilloscope	Tektronix type 422

2 - PURPOSE

- Ensure that the +20 V issued to the controller is maintained within the limits given in the general features (PDS).

3 - PRELIMINARY CHECKS

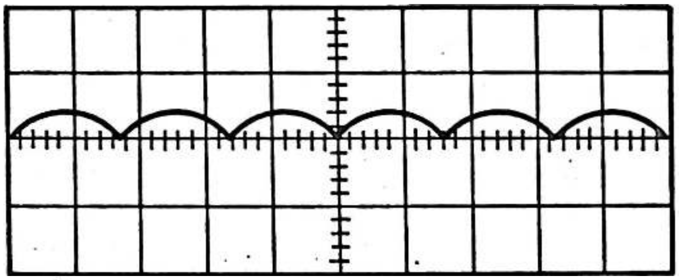
- Check for correct setting of the scope's vertical amplifier.

4 - PROCEDURE

1) - Open the logics module so as to gain access to the P4 +20 V bus bar.

2) - Connect a scope channel to this bus bar and check that the ripple results within a max level of 50mV (refer to fig. 2.2) otherwise, appropriately adjust the main CPU Power Supply.

3) - Set the subsystem to its normal functioning state.



Hor 0.5 μs./cm

Vert. 50 mV/cm

Sync on INT/AUTO/AC

Fig. 2.2. - Ripple Waveform

5 - FINAL CHECKS

- None.

3. CLEANING AND LUBRICATION

ROUTINE : **3.1**

NAME : FAN FILTERS CLEANING

DURATION : 0.1 hr
PREREQUISITES : None

1 - NEEDED MATERIAL

- None.

2 - PURPOSE

- Restore filter efficiency.

3 - PRELIMINARY CHECKS

- None.

4 - PROCEDURE

1) - Switch off the Power Supply.

2) - Remove the following filters:
    - logics module filter
    - adjustment module filters (physically housed on the module covers)
    - transformers module filter (DSC 157 only)

3) - Replace the filters, scrapping the inefficient ones.

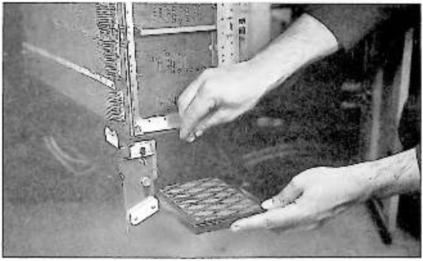


Fig. 3.1. – Logics Module Filter Removal

5 – FINAL CHECKS

- None.

4. ADJUSTMENTS

ROUTINE : 4.1

NAME : ADJUSTMENT OF AN ALI 130/130B OUTPUT

DURATION : 0.2 hr.
PREREQUISITES : The Power Supply and function correctly.

1 - NEEDED MATERIAL

- Oscilloscope	Tektronix type 422	
- Multimeter, class 1.5	P.N.	5282624 A
- Multimeter prods	"	5282628 B
- Open end wrench, 11 mm	"	7133240 T
- Screwdriver, 10 mm	"	0494059 B

2 - PURPOSE

- Adjust the DC output voltage to its nominal value when it results out of the specified PDS limits.

3 - PRELIMINARY CHECKS

- Zero the multimeter and check for correct setting of the scope's vertical amplifier.
- Implement Routine 2.1.
- Take note of the Safety Precautions at Routine 6.3.

4 - PROCEDURE

1) - Gain access to the Power Supply.

2) - Set the load switch jumper straps to the "Internal Load" position (Routine 6.1).

3) - Place the multimeter prods across the involved box voltage sockets. Remember to set the multimeter on the correct DC scale.

- Check that the voltage value results within the following limits:

BOX	NOMINAL VALUE	.SPECS.
± 3	-3 V	-2.88 V to -3.12V
± 3	+3 V	+2.88 V to +3.12V
+ 5	+5.2V	+4.95 V to +5.45V
+ 6	+6 V	+5.75 V to +6.25V
- 36	-36V	-34.55V to -37.45V

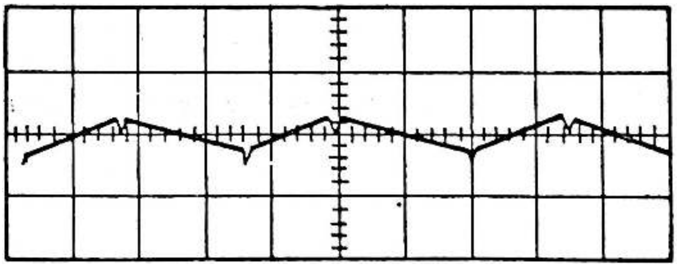
Should this requirement not be met, appropriately rotate either the "VOLTAGE ADJ" or "+3V" or "-3V" pot to obtain the voltage nominal value.

5) - Tighten the appropriate pot lock nut paying attention to hold the voltage at its nominal value.

6) - Connect the scope ground and a channel to the sockets of the involved output voltage box.

- Ripple must result within the max levels specified on the following table and resemble the waveform illustrated in fig. 4.1.

BOX	NOMINAL VOLTAGE	MAX RIPPLE
+ 5	+ 5.2 V	50 mV
+ 6	+ 6 V	50 mV
-36	-36 V	50 mV
± 3	+ 3 V	15 mV
± 3	- 3 V	15 mV



Scale

0,5 μsec/cm - 50 mV/cm

Sync. on INT - AUTO - AC

Fig. 4.1. Ripple Waveform

7) - If the ripple values do not correspond to the given limits, proceed to check the following components:

BOX	NOMINAL VOLTAGE	BOX COMPONENTS	TRANSFORMER PACK COMPONENTS
+5	+ 5.2 V	D 72	D7 to D 12
+6	+ 6V	D 72	D1 to D 6
-36	-36 V	D 72	D36 to D 41
± 3	+ 3 V	-	D13 to D 16
± 3V	- 3 V	-	D17 to D 20

Should this check not satisfy the requirement, replace the involved box as per routine 5.6.

8) - Set the subsystem to its normal functioning state.

5 - FINAL CHECKS

1) - With all the load switch jumper straps set to the "External Load" position, place the multimeter prods (Remember to set the multimeter on the correct DC scale) between ground and sockets "+ 3V", "- 3V", "- 36V", "+6V" (for DSU 160B/C and DSU 110) and "+5V" (for DSU 167 and DSU 157 D/E).

Note

Depending upon the unit under test, the various test points or sockets can be found on:

. the maintenance panel (front side of unit) for DSU 160B
. the rear side of the unit for DSU 160C
. the front side of the unit (ATA 100) for DSU 110
. the rear side of the electronics panel (module A) for DSU 167

For the DSU 157 D/E units, voltage must be measured on the A5H board pin 44 (+ 3V), pin 25 (- 3V), pin 29 (+ 5V), pin 26 (- 36V).

2) - Check that the voltage level is maintained within the specs limits shown in the table at step 4. Otherwise, modify the involved voltage to obtain the required values.

3) - Run through the "DSS Functional Test" diagnostic.

ROUTINE : **4.2**

NAME : -3 V BOX PARALLEL TRANSISTOR CURRENT ADJUSTMENT

DURATION : 0.1 hr
PREREQUISITES : The Power Supply must function correctly

1 - NEEDED MATERIAL

- Multimeter, 1.5 class	P.N. 5282624 A
- Multimeter prods	" 5282628 B
- Open end wrench, 11 mm	" 7133240 T
- Screwdriver 10 mm.	" 0494059 B

2 - PURPOSE

- Set the TR19 current to 2 A.

3 - PRELIMINARY CHECKS

- Zero the multimeter.
- All load switches must be set to the "Internal Load" position.

4 - PROCEDURE

1) - Gain access to the Power Supply.

2) - With the multimeter set to the 1 V DC scale, place the "-" and "+" prods on the "I.C." and ground sockets, respectively.

   - Check the voltage level to be $\boxed{\text{0.2 V}}$ otherwise, appropriately rotate the -3 V box "TR 19 I.C. ADJ." pot to obtain the requirement. Under this condition, a 2 A current will flow on transistor TR 19.

3) - Tighten the adjust pot lock nut.

4) - Set the subsystem to its normal functioning state.

5 - FINAL CHECKS

- Run through the "Functional Test" diagnostic.

ROUTINE : 4.3

NAME : CURRENT PROTECTION ADJUSTMENT (+5 V-12A; -5V -15.5A; +6 V; -36 V)
DURATION : 0.2 hr.
PREREQUISITES : The power Supply must function correctly

1 - NEEDED MATERIAL

- Multimeter, 1.5 class	P.N. 5282624 A
- Multimeter prods	" 5282628 B
- Open end wrench, 11 mm	" 7133240 T
- Screwdriver 10 mm	" 0494059 B

2 - PURPOSE

- Set the current protection working point limit to its nominal value.

3 - PRELIMINARY CHECKS

- Zero the multimeter.
- Take note of routine 6.5.

4 - PROCEDURE

1) - Set the Power Supply switch to OFF.
2) - Set all the load switches to the "Int. Load" position. (Routine 6.1).
3) - Rotate the involved voltage shunt screw fully toward "C.CAL." until the end of run stop.
4) - Rotate the pertinent box "OVERLOAD" pot counterclockwise and set the Power Supply switch to ON.
5) - Adjust the involved box output voltage to its nominal value.

Note

Box +5V output voltage nominal value is:

+5.2 V

6) - Rotate the "OVERLOAD" pot clockwise until the output voltage just TENDS to decrease but not alter its previous voltage level greatly.

7) - Lock the pot in this position and switch off the Power Supply.

8) - Rotate the voltage shunt screw toward "NORM" until the end of run stop and tighten in this position.

9) - Switch on the Power Supply.

10) - Check that the box output voltage corresponds to its nominal value or is lower of 0.1 to 0.2V. Otherwise repeat the routine and try to find the fault causes (box, box boards or shunt).

11) - Implement Routine 4.1.

5 - FINAL CHECKS

- Run through the "Functional Test" diagnostic.

ROUTINE : 4.4

NAME : SLOW VOLTAGE PROTECTION ADJUSTMENT

DURATION : 0.2 hr.
PREREQUISITES : The Power Supply must function correctly.

1 - NEEDED MATERIAL

- Multimeter, 1.5 class	P.N. 5282624 A
- Multimeter prods	" 5282628 B
- Open end wrench, 11 mm.	" 7133240 T
- Screwdriver 10 mm.	" 0494059 B
- Screwdriver 3 mm.	" 4355474 K

2 - PURPOSE

- Adjust the slow voltage protection working point limit to ± 8% of the nominal output voltage value.

3 - PRELIMINARY CHECKS

- Zero the multimeter
- Take note of routine 6.5.

4 - PROCEDURE

1) - Switch off the Power Supply. Set all the load switches to the "Int.Load" position

2) - Turn on the Power Supply and place the meter prods across the pertinent voltage sockets.

3) - Slowly vary the involved box output ("VOLTAGE ADJ.", "+3 V" or "-3V" pot) by first + 8% then - 8% checking that, once these levels are reached (refer to table I), the slow protections cut in to switch off the Power Supply.

- Should the protection limit working points not correspond to those given in table I proceed to step 4 otherwise, go on to step 8.

BOX	NOMINAL VOLTAGE	HIGH PROTECTION LIMIT(+8%)	HIGH PROTECTION LIMIT ADJ.POT	LOW PROTECTION LIMIT(-8%)	LOW PROTECTION LIMIT ADJ.POT
± 3	+ 3 V	+3.24 V	RV11(SEPA)	+2.76 A	RV12 (SEPA)
± 3	- 3 V	-3.24 V	RV10(SEPA)	-2.76 V	RV 9 (SEPA)
- 36	-36 V	-38.9 V	RV8 (SEPA)	-33.1 V	RV 7 (SEPA)
+5 -12A	+5.2V	+5.61 V	RV4(PIPA-A on the left)	+4.78 V	RV3(PIPA-A on the left)
+ 6 (DSC161/162/150)	+6 V	+6.48 V	RV4(PIPA-D)	+5.52 V	RV3(PIPA-D)
+5 -15A DSC 157	+5.2V	+5.61 V	RV4(PIPA-A on the right)	+4.78V	RV3(PIPA-A on the right)

4) Completely rotate the low protection adjust limit pot (high limit for the + 3V) counterclockwise, as required:

RV 7	SEPA	for the - 36V
RV 9	SEPA	for the - 3V
RV11	SEPA	for the + 3V
RV 3	PIPA-A (on the left)	for the + 5V - 12A
RV 3	PIPA-D	for the + 6V (DSC 161/162/150)
RV 3	PIPA-A (on the right)	for the + 5V - 15.5 A (DSC 157)

5) - Completely rotate the high protection adjust limit pot (low limit for the + 3V) clockwise, as required:

RV 8	SEPA	for the - 36V
RV10	SEPA	for the - 3V
RV12	SEPA	for the + 3V
RV 4	PIPA-A (on the left)	for the + 5V - 12A
RV 4	PIPA-D	for the + 6V (DSC 161/162/150)
RV 4	PIPA-A (on the right)	for the + 5V - 15.5A (DSC 157)

6) - To adjust the high protection limit's working point, for anyone of the voltages, proceed as follows:

- Vary the involved box voltage by + 8% (refer to table I)
- Referring to table I, slowly rotate the relative protection adjust pot countercloclwise (clockwise for the + 3V) until Power Supply switch off.
- Slightly decrease the output voltage by rotating the appropriate box pot counterclockwise.
- Switch-on the Power Supply and, increasing the output voltage, check the threshold.
  Should it not correspond to the specified requiremens, adjust the protection pot to obtain the correct working point limit.
- Restore the output voltage to its correct value.

7) - To adjust the low protection limit's working point, for anyone of the voltages, proceed as follows:

- Vary the involved box voltage by - 8% (refer to table I)
- Referring to table I, slowly rotate the relative protection adjust pot clockwise (counterclockwise for the + 3V) until Power Supply switch-off.
- Slightly increase the output voltage by rotating the appropriate box pot clockwise.
- Turn on the Power Supply and, decreasing the output voltage, check the threshold.
- Should it not correspond to the specified requirements, adjust the protection pot to obtain the correct working point limit.

8) - Restore the box output voltage to the nominal value.

> **Note**
>
> Box + 5V output voltage nominal value:
>
> + 5.2 V

9) - Tighten the pots lock-nuts.

10) - Implement Routine 4.1.

5 - FINAL CHECKS

- Run through the "Functional Test" diagnostic.

ROUTINE	: **4.5**
NAME	: "ALER" SIGNAL ADJUSTMENT (Board COMA)
DURATION	: 0.2 h
PREREQUISITES	: Routine 2.2

1 – NEEDED MATERIAL

– Oscilloscope	Tektronix type 422
– Screwdriver, 3 mm	P.N. 4355474 K

2 – PURPOSE

– Ensure that logic signal "ALER" (issued to the controller) switches when the +20 EXT no longer results within the ± 8% tolerance limits.

3 – PRELIMINARY CHECKS

– Ensure for correct setting of the vertical scope amplifier.

4 – PROCEDURE

1) – Switch on any unit and wait for heads to load.

2) – Gain access to the Power Supply.

3) – Rotate pot RV1 completely counterclockwise and RV2 completely clockwise. These pots are physically located on board COMA.

4) – Connect a scope channel on controller loc. C14-01 (ALER) and check that, with the Power Supply switched on, the monitored signal results $\boxed{+10\ \text{V}}$ approximately with no peak toward "0 V".

5) – Increase the CPU +20 V by +8 % setting it to +21.6 V.

Note

The CPU +20 voltage protection working point limits are set to ± 10%.
The voltage variations required in steps 5 and 7 should not therefore call into action this protection.
If however it should be called upon, before continuing with this procedure, proceed to reset the working point limits.

6) - Rotate board COMA pot RV1 clockwise until the scope monitored signal falls to 0 V, or signals peaks toward "0V".

7) - Decrease the CPU +20 V by -8 %, setting it to +18.4 V.

- Check that the monitored signal results $\boxed{\text{+10 V approx.}}$

8) - Rotate board COMA pot RV2 counterclockwise until the monitored signal (ALER) falls to 0 V, or signals peaks toward "0V".

9) - Restore the CPU +20 V to its nominal value once more and check that signal ALER passes to +10 V.

10) - Set the subsystem to its normal functioning state.

5 - FINAL CHECKS

- Run through the "Functional Test" diagnostic.

5. REMOVALS AND REPAIRS

ROUTINE : **5.1**

NAME : GUD 030-GUD 040 BOARD REPAIR and REPLACEMENT

DURATION : -

PREREQUISITES : See Note①(DSC 161-162/150) and Note 2 (DSC 157)

Note ①

In case of board repair or replacement, on the GUD 030, consult the following documentation :

- GUD 030 Isolation Test	(See DSS 110/161/162/150-Vol.1)
- FAULT Chart	(See DSS 110/161/162/150-Vol.2)
- Package Replacement Procedure	(See DSS 110/161/162/150-Vol.2)
- Board Tester Operating Instructions	(See G 120/130 - CPU-Vol.5)

Note ②

In case of board repair or replacement, on the GUD 040, consult the following documentation :

- GUD 040 Isolation Test	(See DSS 157 - Vol. 1)
- FAULT Chart	(See DSS 157 - Vol. 2)
- Package Replacement Procedure	(See DSS 157 - Vol. 2)
- Board Tester Operating Instructions	(See G 120/130 CPU vol. 5)

ROUTINE : 5.2
NAME : VAR 585 FAN REPLACEMENT
DURATION : 0.5 hr
PREREQUISITES : Routine 6.3

1 - NEEDED MATERIAL

- Socket spanner, 5.5 mm (7/32")	P.N. 4355531 L
- Soldering iron	" 7144451 X
- Solder	" 6138215 L
- Screwdriver 10 mm.	" 0494059 B
- Fan	See catalog

2 - PURPOSE

- Replace a faulty VAR 585 fan.

3 - PRELIMINARY CHECKS

- None.

4 - PROCEDURE

1) - Set the Power Supply OFF.

2) - Swing out the logics module.

3) - Loosen the 4 knurled screws fixing the fan group to the lower part of the module.
Extract the group by exerting pressure in direction of the chassis swing out hinges.

4) - Remove the wiring connector.
The group is now completely free.

5) - Using the 5.5 mm (7/32") socket spanner, remove the 4 nuts holding the faulty fan and extract it.

6) - Unsolder the supply wires and solder them onto the new fan.

7) - To reassemble, repeat steps 5 through 1, carrying out the operations in the opposite manner.

5 - FINAL CHECKS

- Check fan efficiency.
- Set the subsystem to its normal functioning state.

ROUTINE : 5.3

NAME : VAR 585 THERMOSWITCH REPLACEMENT

DURATION : 0.5 hr
PREREQUISITES : Routine 6.3

1 - NEEDED MATERIAL

- Screwdriver	P.N. 4355474 P
- Soldering iron	" 7144451 X
- Solder	" 6138215 L
- Screwdriver	" 0494059 B
- Thermoswitch support	See catalog

2 - PURPOSE

- Replace a faulty VAR 585 thermoswitch.

3 - PRELIMINARY CHECKS

- None.

4 - PROCEDURE

1) - Carry out routine 5.2 steps 1 to 4.
2) - Remove the 2 screws holding the protection group to be replaced.
3) - Unsolder the thermoswitch connections.
4) - Remove the resistor and support to cover fixing screws.
5) - Extract the faulty thermoswitch support and insert the new one in place.
6) - Replace and tighten the resistor/support to cover fixing screws.
7) - Solder the 2 leadwires on the new thermoswitch.
8) - Tighten the new protection group in place with the appropriate fixing screws.
9) - Reassemble the VAR 585, carrying out the removal operations in the reverse order.
10) - Set the Power Supply ON.

5 - FINAL CHECKS

- None.

ROUTINE : **5.4**

NAME : ALI 130/ALI 130B FANS REPLACEMENT

DURATION : 0.5 hr
PREREQUISITES : Routine 6.3

1 - NEEDED MATERIAL

- Curved nose pliers	P.N.	7137593 Y
- Soldering iron	"	7144451 X
- Solder	"	6138215 L
- Tweezers	"	7137380 A
- Screwdriver	"	0494059 B
- Fans		See catalog

2 - PURPOSE

- Replace any faulty ALI 130/ALI 130B fan.

3 - PRELIMINARY CHECKS

- None.

4 - PROCEDURE

1) - Set the Power Supply switch to OFF.
2) - Remove the adjustment pack covers, in case of pertinent fan replacement, or (for DSC 157 only) extract the transformers pack filter to replace the relative fan.
3) - Unsolder the fan's red and black leadwires.
4) - Remove the 4 screws fixing the fan support to the S.M.N. module.
5) - Extract the group, remove the protection grate and replace the faulty fan.
6) - Replace the protective grate and restore the subsystem to its normal functioning conditions.

5 - FINAL CHECKS

- Check filters state and, if necessary, replace them as per routine 3.1.
- Check fan efficiency.

ROUTINE : **5.5**

NAME : ALI 130/ALI 130B BOARDS REPLACEMENT

DURATION : -
PREREQUISITES : Routine 6.3.

1 - NEEDED MATERIAL

- Oscilloscope	Tektronix type 422
- Screwdriver	P.N. 0494059 B

2 - PURPOSE

- Replace any faulty ALI 130/ALI 130B boards (AMER- CIBO- COMA- PIPA- SEPA).

3 - PRELIMINARY CHECKS

- The load switches must be set to the "Internal Load" position.Refer to routine 6.1.
- Take note of routine 6.5.

4 - PROCEDURE

1) - Switch-off the Power Supply.

2) - Remove the involved board's plastic protection. Extract the board and insert the new one.

3) - Switch-on the Power Supply and proceed with :

- Step 4 in case of CIBO-A-E-D boards replacement
- Step 5 in case of AMER board replacement
- Step 6 in case of PIPA-A or PIPA D or SEPA boards replacement.
- Step 7 in case of COMA board replacement

4) - Connect the scope on test point "B" of the new CIBO board and check for a waveform as illustrated in fig. 5.1.

- Should the spread not result within $\boxed{150 \text{ to } 300\ \mu s}$ place a 2.7 KpF - 200 V capacitor (P.N. 5011825 M) in loc. C19.
- Implement routines 4.1 and 4.3, carrying out those steps that interest the involved box.
- Proceed with step 8.

5) - In case of an AMER board replacement, implement routines 4.1 and 4.2, carrying out those steps involving the ± 3 V box.

- Proceed with step 8.

6) - In case of a PIPA-A or PIPA-D or SEPA board replacement, implement routines 4.1. and 4.4, carrying out those steps that interest the involved board.

- Proceed with step 8.

7) - In case of a COMA board replacement, carry out routine 4.5.

8) - Set the subsystem to its normal functioning state.

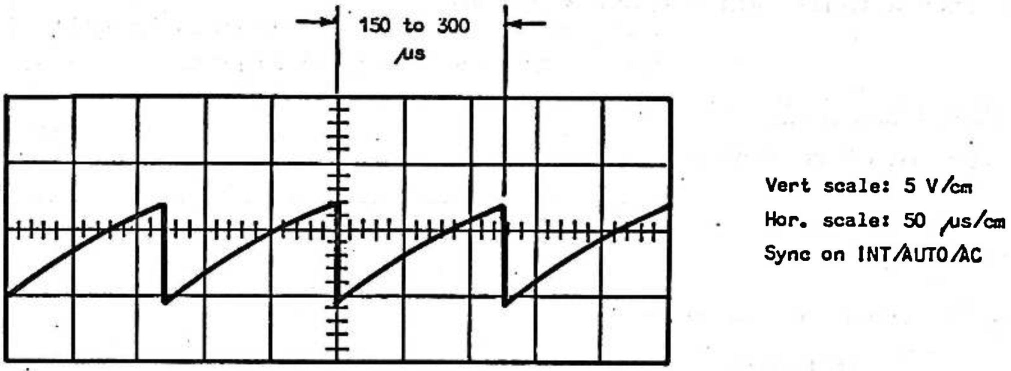


Fig. 5.1. - Waveform Monitored on PWB CIBO Test Point "B"

5 - FINAL CHECKS

- Run through the "Functional Test" diagnostic.

ROUTINE : **5.6**
NAME : ALI 130/ALI 130B SUPPLY BOX REPLACEMENT
DURATION : -
PREREQUISITES : Routine 6.3

1 - NEEDED MATERIAL

- Allen Key, 8 mm	P.N. 7133170 U

2 - PURPOSE

- Replace a faulty ALI 130/ALI 130B box.

3 - PRELIMINARY CHECKS

- Take note of routine 6.5.

4 - PROCEDURE

1) - Set the Power Supply OFF.
2) - Swing out the controller's logic panel.
3) - Disassemble the box to be replaced by loosening the fixing screw on the corresponding connector.
4) - Remove the CIBO or AMER board from the faulty box and replace it on the new one.
5) - Mount the box in place and tighten the fixing screw on the corresponding connector.
6) - Set all the load switches to their "Internal Load" position.
7) - In case of a ± 3 V box replacement, implement routines 4.1 and 4.2 carrying out only those steps involving this box.
8) - In case of a +5 V, +6 V (DSC 161-162/150 only) or -36V box replacement, implement routine 5.5 step 4 and routines 4.1 and 4.3, only carrying out those steps which interest the involved box.
9) - Restore the subsystem to its normal functioning state.

5 - FINAL CHECKS

- Run through the "Functional Test" diagnostic.

ROUTINE : **5.7**

NAME : REPLACEMENT OF ALI 130/ALI 130B COMPONENTS

DURATION : -
PREREQUISITES : Routine 6.3

Note

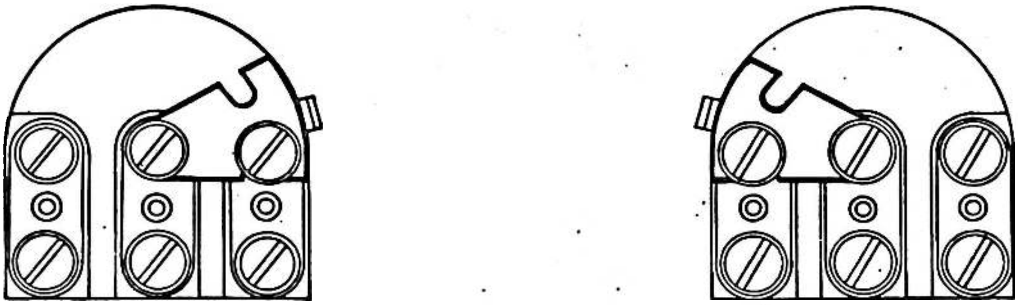
Possibility of replacing any component has been foreseen. However always consult the machine documentation and check those adjustments which are subject to change as a consequence of the replacement.

6. MAINTENANCE AIDS

ROUTINE : 6.1
NAME : LOAD SWITCHES
DURATION : -
PREREQUISITES : Routine 6.3

To avoid damaging the utilizing circuits, the ALI 130/ALI 130B has also been fitted with an internal dummy load circuit.

To transfer over to this circuit, position all the pertinent switch jumper straps to the Internal Load position. Refer to fig. 6.1.



Jumper strap set to External Load position

Jumper strap set to Internal Load position

Fig. 6.1. - ALI 130 Load Switches

The Internal Load switch transfer operation must always be accomplished with the machine switched off.
This holds true for any ALI 130/ALI 130B check, adjustment, or repair procedure that is to be implemented.

ROUTINE : 6.2

NAME : TEMPORARY EXCLUSION of the + 5; +6 (DSC161-162-150 only); - 36 V FAST VOLTAGE PROTECTION

DURATION : -
PREREQUISITES : Routine 6.3

1 - NEEDED MATERIAL

- Jumper P.N. 0837137 Y

2 - PURPOSE

- To enable the execution of certain checks, avoiding Power Supply switch-off

3 - PRELIMINARY CHECKS

- The load switches must be set to the "Internal Load" position. See routine 6.1.

4 - PROCEDURE

1) - Gain access to the ALI 130/ALI 130B.
2) - Set the ALI 130/ALI 130B switch to OFF.
3) - Insert a jumper between board CIBO sockets "G" and "H". The said board is located in the pertinent voltage box, under test.
4) -.Carry out the necessary check routine.
5) - Remember that upon completion of the check, the jumper MUST BE REMOVED.

5 - FINAL CHECKS

- Run through the "Functional Test" diagnostic.

ROUTINE	: **6.3**
NAME	: SAFETY PRECAUTIONS
DURATION	: -
PREREQUISITES	: None

All areas that present hazards and consequent foreseeable injuries to persons, such as :

- High voltage areas
- High temperature zones
- High energy potential points
- Moving parts

have been appropriately protected and, in some cases, bear warning labels. Engineers are therefore recommended to take maximum precaution to avoid any personal accidents when having to service the subsystem without these protections.

Upon completion of the operations therefore, replacement of the protection is a MUST.

ROUTINE : **6.4**

NAME : READ/WRITE TIMINGS CHECK

DURATION : –
PREREQUISITES : None

The following two timing charts have been inserted as reference to help resolve doubts that may arise from the read chain and the write oscillator.

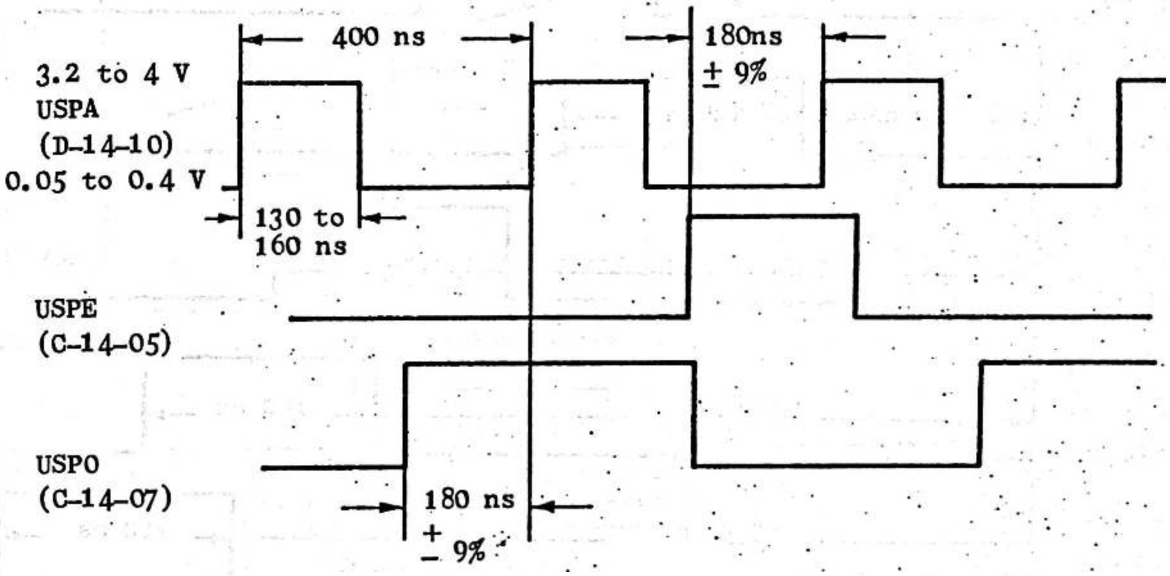


Fig. 6.2. – Write Oscillator (PWB TERE)

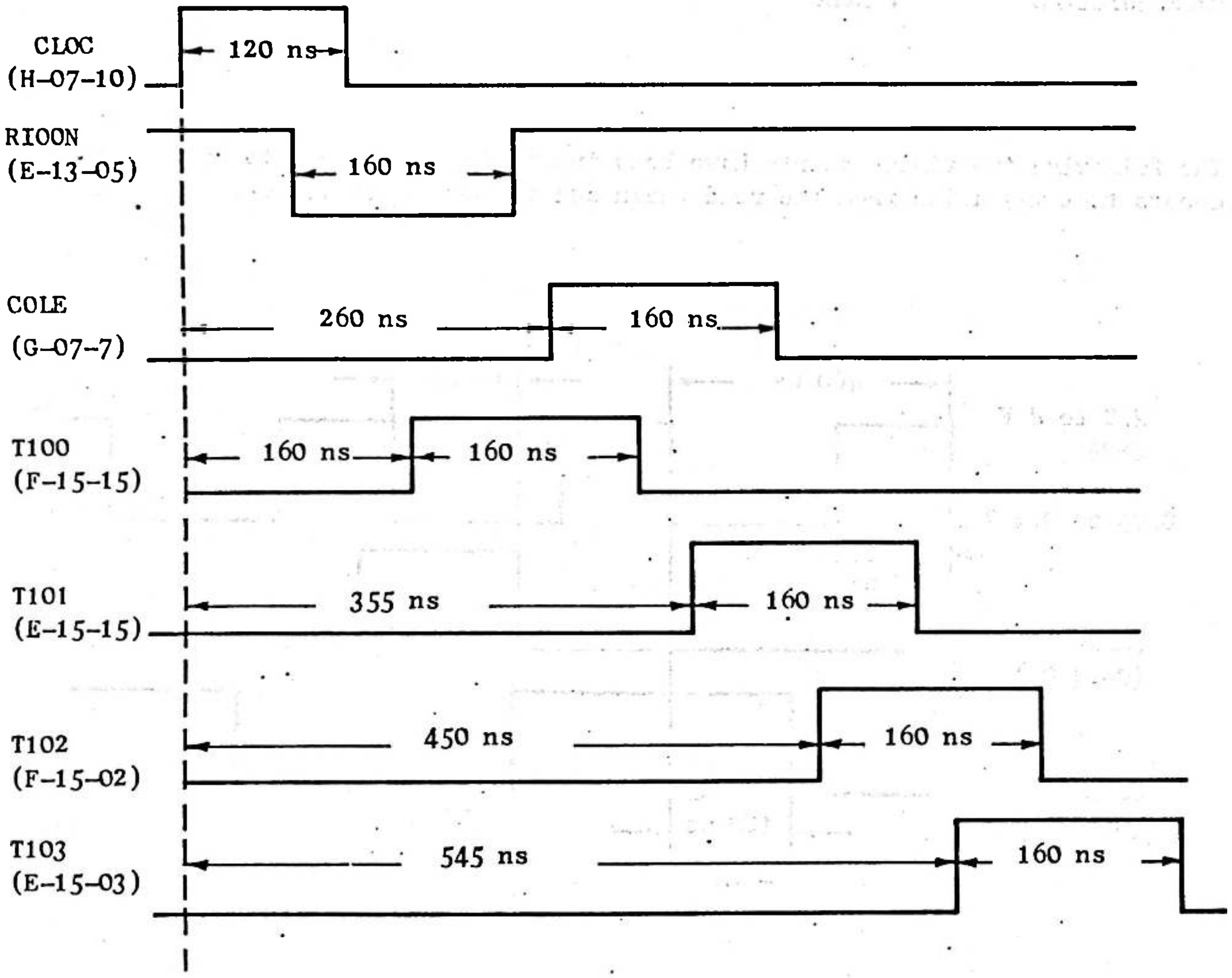


Fig. 6.3. – LIRI 2A SPIL 2A Timings

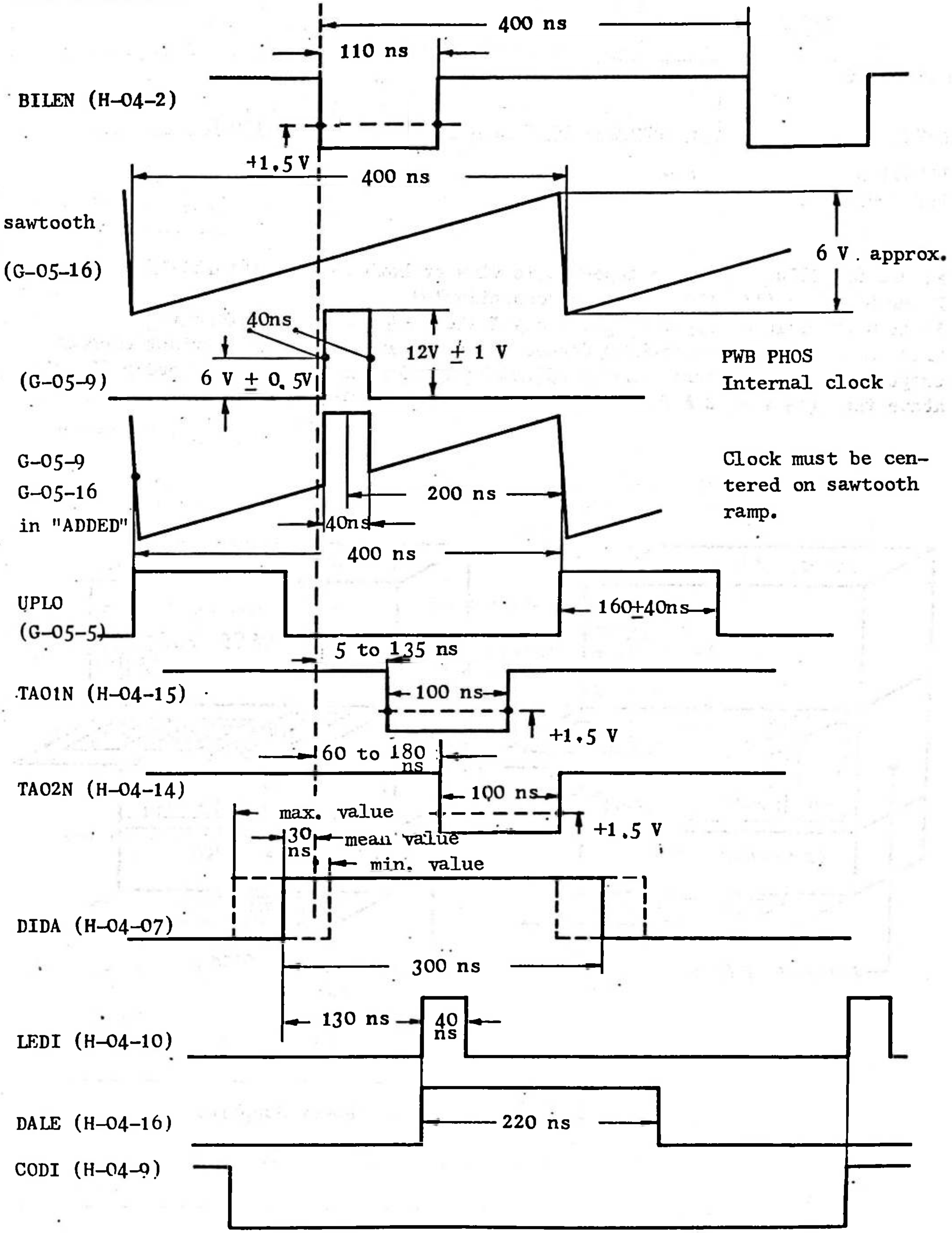


Fig. 6.4. - PHOS-D RIRI-2A Timings

ROUTINE : **6.5**

NAME : TOPOGRAPHIC VIEW of ALI 130 and ALI 130 B

DURATION : -
PREREQUISITES : None

Figure 6.5 illustrates the topographic view of both the DSC 161-162-150 and DSC157 Power Supplies (ALI 130 and 130 B respectively).
It is worthwhile noting that the two ALI 130 B +5 V boxes (differently named in this manual and on the machine documentation because of their distinct current output) have their corresponding adjust boards located in the same order directly above them (+5 V - 12 A PIPA-A before +5 V - 15.5A PIPA-A).

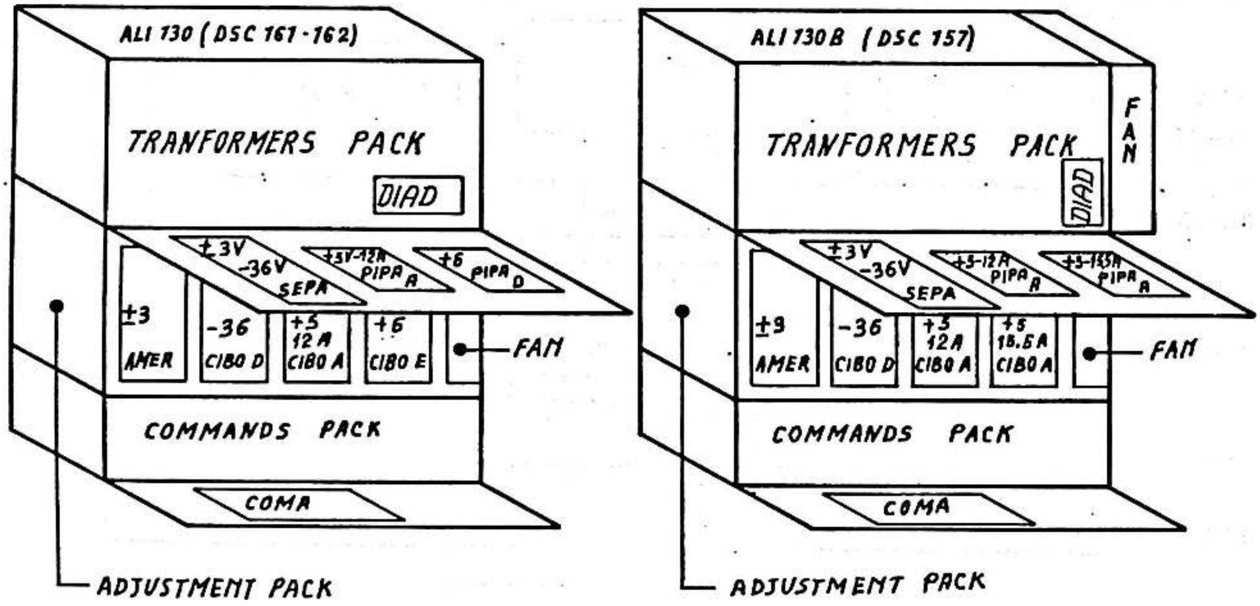


Fig. 6.5. - ALI 130 and 130 B Power Supplies

MAINTENANCE SCHEDULE TYPE H

DSU 167

SPECIAL TOOLS			
	. Cleaning paddle	P/N	4370807 V
	. Disc unit cleaner	P/N	5670107 G

MACHINE OFF OPERATIONS

1. CLEANING

a- Read the notes listed on the Preventive Maintenance Log

b- check that the operator has cleaned :

- the dispac loading area
- the transparent cover

c- clean and check :

- head surfaces (3.1.)
- electronics pack air filters (3.2.)

2. SCHEDULED REPLACEMENTS

According to the Preventive Maintenance Log checked, if necessary replace :

- ext. air intake filter.

3. CHECKS

a- Check for absence of oil leaks on the hydraulic circuit (fluid-tight gaskets, belt and pump pulley) (3.3.)

b- check oil catcher's level (3.4.)

4. LUBRICATION

Lubricate as per Lubrication Plan:

a- Drives Without Felt Wicks

- grease carriage pinions, rack gear and detent gear (3.5.)

b- Drives Fitted With Felt Wicks

- oil the felt wicks and grease the detent gear (3.5.)

c- carriage roller-way planes (3.6.)

d. spindle threads and outer cone surface (3.7.)

e- head loading linkage pivots (3.8.)

f- head loading cam (3.9.)

MACHINE ON OPERATIONS

5. FUNCTIONAL CHECKS

Remove the top cover and check :

a- that the disc cleaning brushes are submitted to a sufficient physical compression (index of wear) and that they result free from oxide traces (otherwise, replace them)

b- that the heads fly correctly over the dispac surfaces

c- replace the cover and feed through a Unit Test diagnostic.

6. FINAL PROCEDURES

Fill-in the Preventive Maintenance Log and possible service report card.

Note

Reference numbers, in brackets, refer to the DSU 167 Maintenance Manual code 59A301558.
The pertinent Preventive Maintenance Log has code 4.033.4.081.0/A and it refers to all 3 spindles A-B and C.

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MAINTENANCE SCHEDULE TYPE F   DSU 167

SPECIAL TOOLS		
	. Cleaning paddle	P/N 4370807 V.
	. Disc unit cleaner	P/N 5670107 G

MACHINE OFF OPERATIONS

1. CLEANING

a- Read the notes listed on the Preventive Maintenance Log

b- check that the operator has cleaned :
- the dispac loading area
- the transparent cover

c- clean and check :
- head surfaces (3.1.)
- electronics pack air filters (3.2.)

2. CHECKS

a- Check for absence of oil leaks on the hydraulic circuit (fluid-tight gaskets, belt and pump pulley) (3.3.)

b- check oil catcher's level (3.4.)

3. LUBRICATION

Lubricate as per Lubrication Plan:

a- Drives Without Felt Wicks
- grease carriage pinions, rack gear and detent gear (3.5.)

b- drives Fitted With Felt Wicks
- oil the felt wicks and grease the detent gear (3.5.)

c- carriage roller-way planes (3.6.)

d- spindle threads and outer cone surface (3.7.)

e- head loading linkage pivots (3.8.)

f- head loading cam (3.9.)

MACHINE ON OPERATIONS

4. FUNCTIONAL CHECKS

Remove the top cover and check :

a- That the disc cleaning brushes are submitted to a sufficient physical compression (index of wear) and that they result free from oxide traces (otherwise, replace them)

b- that the heads fly correctly over the dispac surfaces

c- Replace the cover and feed through a Unit Test diagnostic.

5. FINAL PROCEDURES

Fill-in the Preventive Maintenance Log and possible service report card.

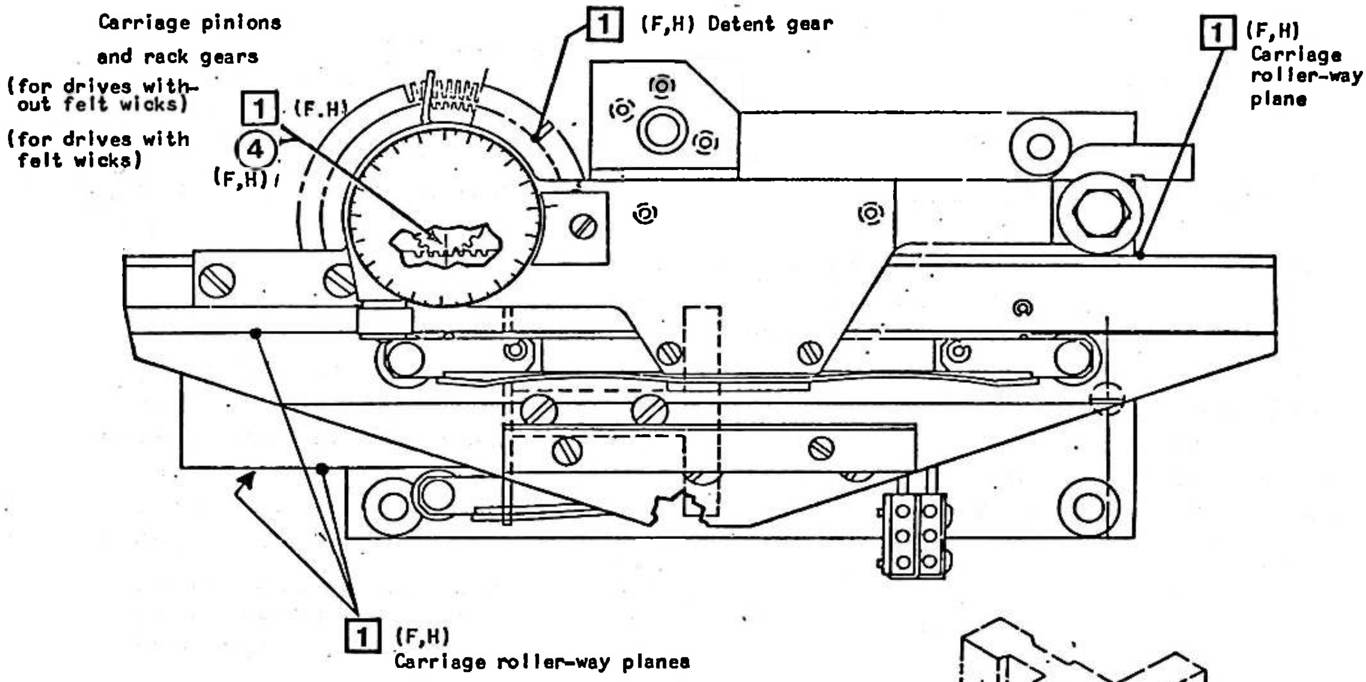
Note

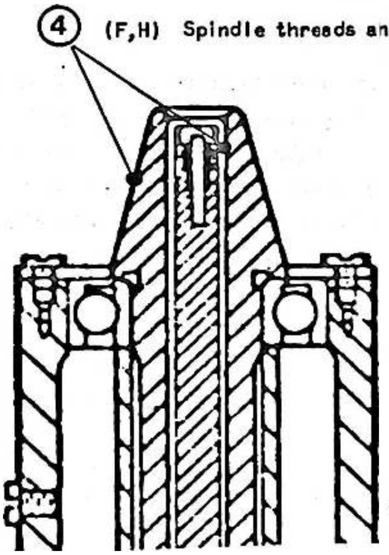
Reference numbers, in brackets, refer to the DSU 167 Maintenance Manual code 59A301558. The pertinent Preventive Maintenance Log has code 4.033.4.681.0/A and it refers to all 3 spindles A-B and C.

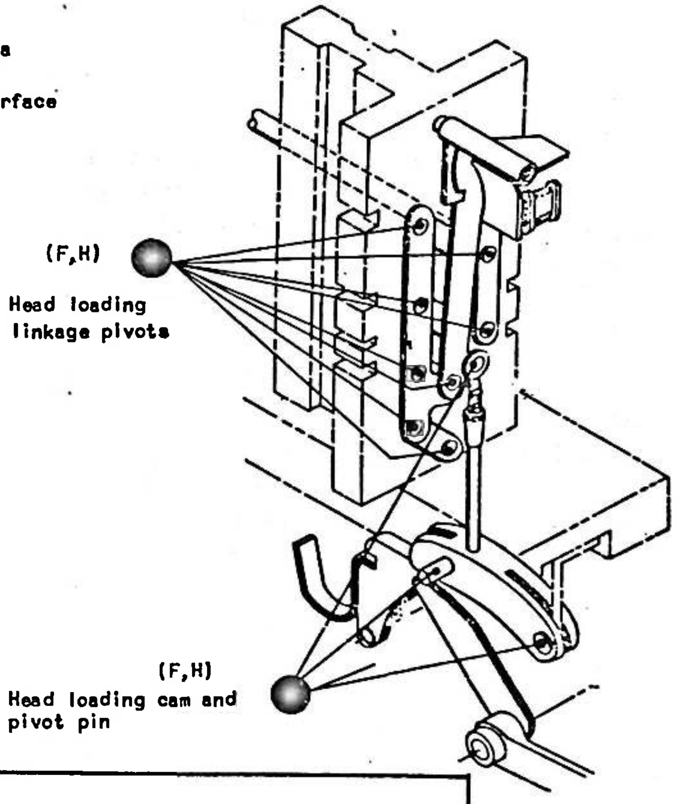
LUBRICATION PLAN

DSU 160C 162 167

LUBRICANT TYPES			
	●	Hydraulic oil	P.N. 0491026 N
	④	Heavy duty oil	P.N. 0491012 E
	1	Multi purpose grease	P.N. 0491014 D


Carriage pinions and rack gears
(for drives without felt wicks)
1 (F,H)
(for drives with felt wicks)
④ (F,H)
1 (F,H) Detent gear
1 (F,H) Carriage roller-way plane
1 (F,H) Carriage roller-way planes





Note
Letters, in brackets, refer to the pertinent Maintenance Schedule.
Standard lubricants have been foreseen. Quantity ● ☐ - Little ◉ ⧈ = average.

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MAINTENANCE SCHEDULE TYPE F
DSU 157 D

REQUIRED MATERIAL		
	. Cleaning Paddle	P/N 4370807 V
	. Dental mirror	" 7137830 Y
	. Disc unit cleaner	" 5670107 G
	. Chammy leather	" 3583900 W

MACHINE OFF OPERATIONS

1 - CLEANING

a- Read the notes reported on the Preventive Maintenance Log (No. 4.033.4.207.1/A)

b- verify that the shroud has been cleaned by the operator otherwise, proceed to clean it with disc unit cleaners and remove any possible loose metal or dust particles using the sticky surface of an adhesive tape or suchlike

c- thoroughly clean the female cone interior threads which engage the lock-shaft and, using a dry chammy cloth, proceed to clean the spindle cone.

d- using disc cleaner wipers, thoroughly clean the read/write heads ascertaining that they are free of oxide build-ups, stains or scratches (dental mirror).

2 - CHECKS

a- Check that the disc cleaning brushes result free of oxide traces otherwise, replace them

b- load a scratch dispac and, manually moving the brushes into the pac, check that they are submitted to a sufficient physical compression (index of wear) otherwise, replace them.

c- check that both the sector block and spindle detent operate correctly when opening and closing the glass cover. No interference should be witnessed and verify that the spindle detent perfectly enters in the appropriate spindle notch

d- Verify that the static discharge contact is correctly aligned with the spindle shaft.

3 - LUBRICATION

According to the appropriate Lubrication Plan proceed to :

a- apply a thin coat of oil on the dispac lock-shaft threads. Remove any excess oil

b- apply a thin coat of oil on the lower rackgear. While holding the track indicator fixing nut firm, remove the screw and fill-up the underlying oil deposit. Replace the screw ascertaining that the track indicator has not moved. Manually move the carriage, removing any excess oil deposited on the rackgears.

MACHINE ON OPERATIONS

4 - FUNCTIONAL CHECKS

a- Check that all fans rotate correctly.

b- Verify that all operator panel and Fault Panel indicators light-up. Replace any faulty lamps.

c- Load a dispac and check that no head to disc interference occurs.

5 - FINAL OPERATIONS

a- Run the functional test diagnostic with a dispac already formatted on another unit (compatibility test)

b- Fill-in the Preventive Maint. Log (No.4.033.4.207.1/A) and possible service report card.

MAINTENANCE SCHEDULE TYPE H

DSU 157 D

REQUIRED MATERIAL	. Cleaning paddle	P/N 4370807 V
	. Dental mirror	" 7137830 Y
	. Disc unit cleaner	" 5670107 G
	. Chammy leather	" 3583900 W

MACHINE OFF OPERATIONS

1 - CLEANING

a- Read the notes reported on the Preventive Maintenance Log. (No. 4.033.4.207.1/A)

b- verify that the shroud has been cleaned by the operator otherwise, proceed to clean it with disc unit cleaners and remove any possible loose metal or dust particles using the sticky surface of an adhesive tape or suchlike

c- Thoroughly clean the female cone interior threads which engage the lock-shaft end, using a dry chammy cloth, proceed to clean the spindle cone.

d- using disc cleaner wipers, thoroughly clean the read/write heads ascertaining that they are free of oxide build-ups, stains or scratches (dental mirror).

2 - SCHEDULED REPLACEMENTS

According to the appropriate Preventive Maint.Log, proceed to replace the air intake filter.

3 - CHECKS

a- Check that the disc cleaning brushes result free of oxide traces otherwise, replace them

b- load a scratch dispac and, manually moving the brushes into the pac, check that they are submitted to a sufficient physical compression (index of wear) otherwise, replace them.

c- Check that both the sector block and spindle detent operate correctly when opening and closing the glass cover. No interference should be witnessed and verify that the spindle detent perfectly enters in the appropriate spindle notch.

d- verify that the static discharge contact is correctly aligned with the spindle shaft

e- check the drive belt's state of wear and, if necessary, replace it.

4 - LUBRICATION

According to the appropriate Lubrication Plan proceed to :

a- apply a thin coat of oil on the dispac lock-shaft threads. Remove any excess oil

b- apply a thin coat of oil on the lower rackgear. While holding the track indicator fixing nut firm, remove the screw and fill-up the underlying oil deposit. Replace the screw ascertaining that the track indicator has not moved. Manually move the carriage, removing any excess oil deposited on the rackgears

c- lubricate the spindle detent fulcrum pin and the various points of friction on the relative thrust mechanism.

MACHINE ON OPERATIONS

5 - FUNCTIONAL CHECKS

a- Check that all fans rotate correctly

b- verify that all operator panel and Fault Panel indicators light-up. Replace any faulty lamps

c- load a dispac and check that no head to disc interference occurs.

6.- FINAL OPERATIONS

a- Run the functional test diagnostic with a dispac already formatted on another unit (compatibility test)

b- fill-in the Preventive Maint. Log (No.4.033.4.207.1/A) and possible service report card.

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PREVENTIVE MAINT. LOG

DSU 167

YEAR MACHINE TYPE and SERIAL No.

MAINTENANCE TYPE	**F**	
Approx. duration 2 h.h/10		
FREQ.	2 months	3 months
SHIFTS	3	1-2

SCHED. DATE	EFFECT. DATE	EFFECT. DURAT.	ENGR.

MAINTENANCE TYPE	**H**	
Approx. duration 2,3 h.b/10		
FREQ.	6 months	Yearly
SHIFTS	2-3	1

SCHED. DATE	EFFECT. DATE	EFFECT. DURAT.	ENGR.

Note

The maintenance schedules are referred to all 3 spindles A-B and C.
Should it occur that maintenance operations have to be interrupted (because of customer exigencies, etc.) remember to record the event on te service report, "NOTES" section, registering the spindle (corrisponding letter) on which maintenance has already been effected.

PIECE	REPL. FREQ. (hours)	SCHEDULED REPLACEMENTS					
Ext. air filter P/N 4368228 P	Every Prev. Maint. "H"						

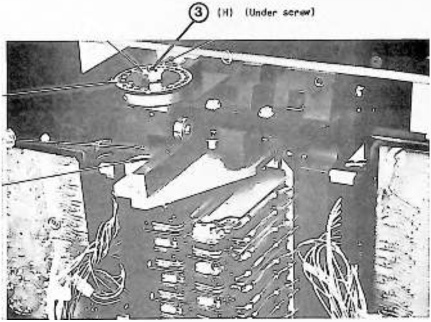
DATE	NOTES

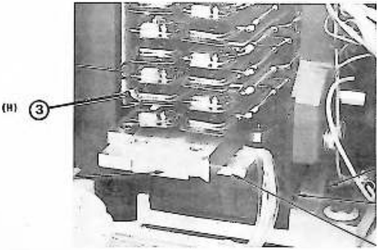
Mod. 0146

LUBRICATION PLAN

DSU 157 D

REQUIRED	. Medium Oil ③	P/N 0491020 G
MATERIAL	. Open end wrench-7/16"	P/N 7133413





Note

Letters in brackets recall the pertinent Maintenance Schedule

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PREVENTIVE MAINT. LOG

DSU 157 D

YEAR	MACHINE	TYPE AND SERIAL NUMBER

MAINTENANCE TYPE **F**
Approx. duration 0.9 h.h/10

FREQ.	2 months	3 months
SHIFTS	3	1-2

SCHED. DATE	EFFECT. DATE	EFFECT. DURAT.	ENGR.

MAINTENANCE TYPE **H**
Approx. duration 1.1 h.h/10

FREQ.	6 months	Yearly
SHIFTS	2-3	1

SCHED. DATE	EFFECT. DATE	EFFECT. DURAT.	ENGR.

PIECE	REPL. FREQ. (hours)	SCHEDULED REPLACEMENTS					
Air intake filter	Every Prev. Maint. "H"						
(P/N 03630015-001)							

DATE	NOTES

Mod. 0146

PARTS

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GOVERNO DI MEMORIA A DISCHI

DSC 161/162/157/150

Catalogo parti di ricambio

SECONDA EDIZIONE

Edito a cura della
Sezione Assistenza Tecnica

4.813.5.001.1

LIVELLO DI EVOLUZIONE

Nº AGG.	PAGINE INTERESSATE	DATA
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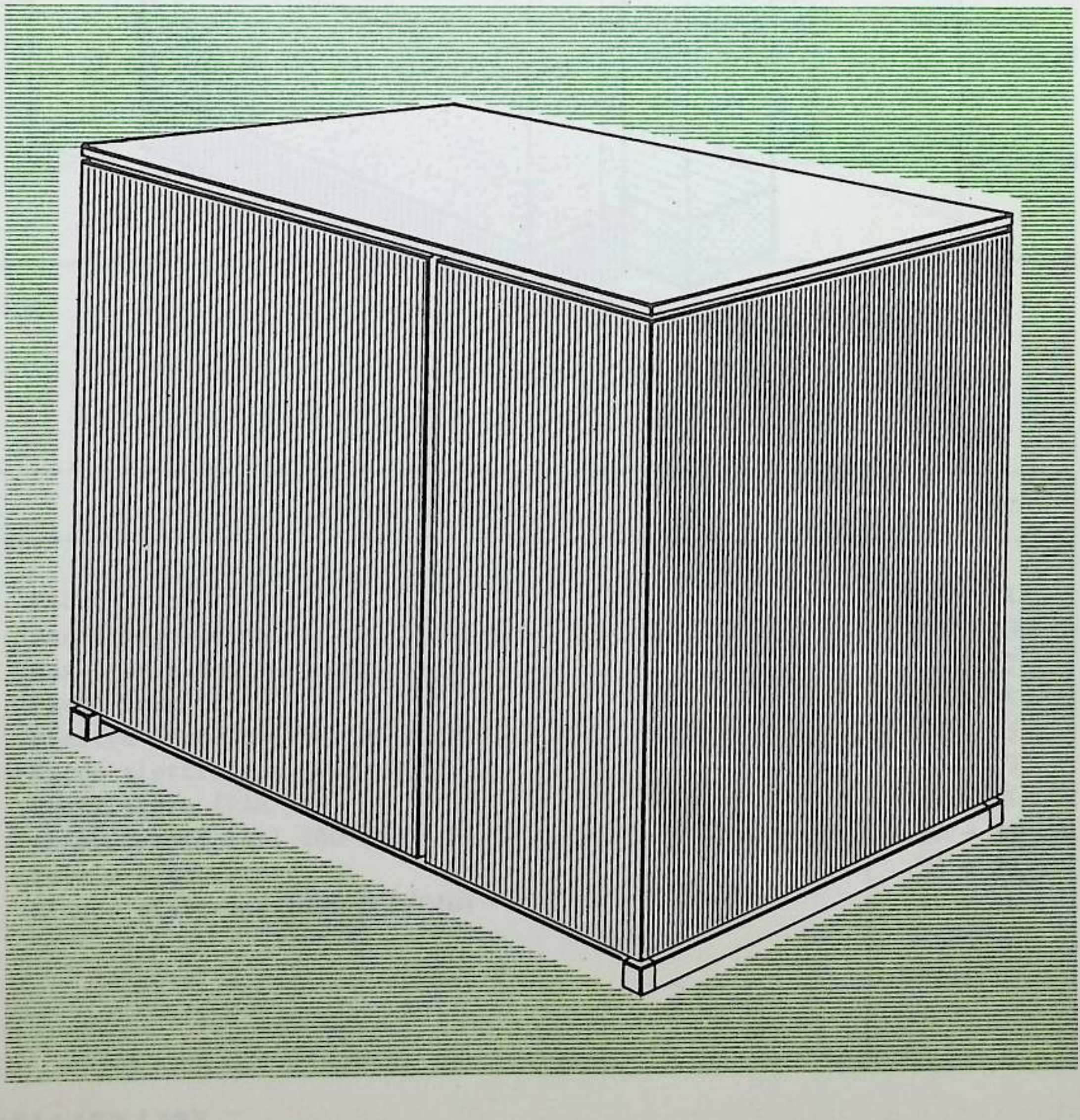
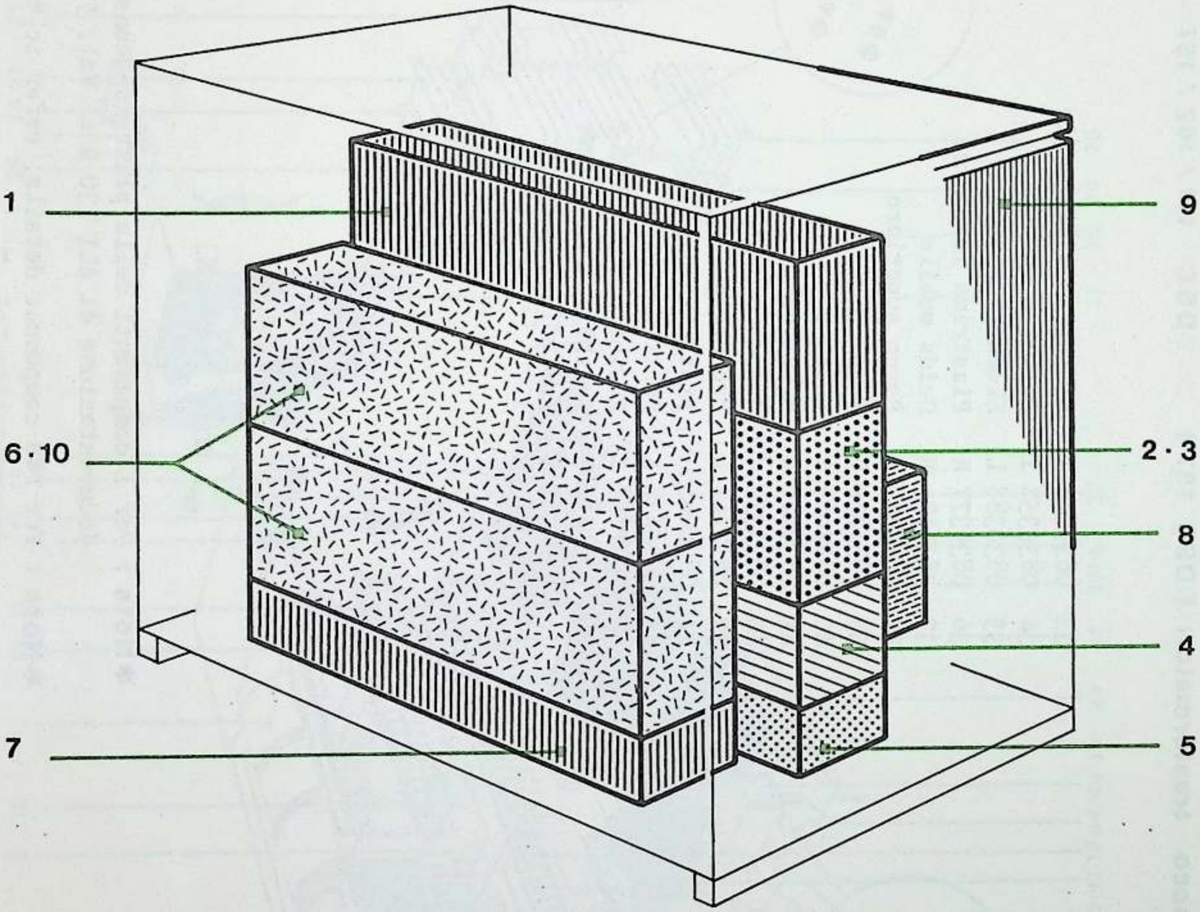


TAVOLA DI RIFERIMENTO



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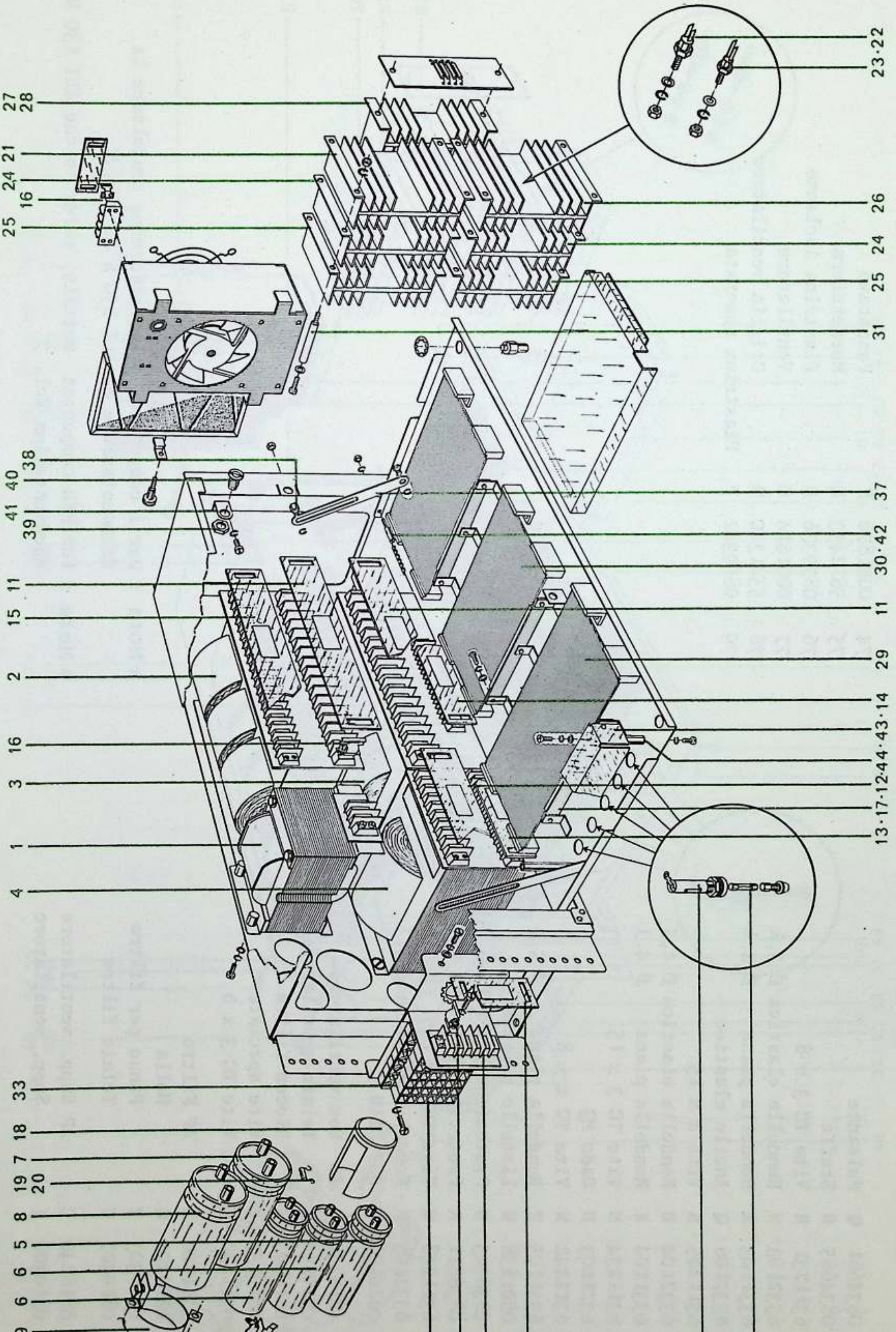
1	5621016	G	Induttanza 10 mH
2	5445095	F	Trasformatore T 4000/32/26
3	5445098	C	Trasformatore T 4000/32/27
4	5445093	T	Trasformatore T 4000/22/20
5	5045550	T	Condensatore 2500 µF 75VL
6	5038680	C	Condensatore 6000 µF 25VL
7	5035825	Q	Condensatore 21000 µF 15 VL
8	0001234	X	Condensatore 11000 µF 25 VL
9	0002138	H	Fascetta TP 1462
10	0001402	S	Fascetta TP 1420
11	0839367	Q	Piastrina
12	0839360	E	Piastrina
13	0839344	A	Piastrina
14	0839348	B	Piastrina
15	0839353	N	Piastrina
16	0839653	U	Molletta TP A
17	0620233	Z	Piastrina COSE
18	0837218	M	Protezione cond.
19	4934527	T	Resistenza 3,3 KΩ 0,5 W 2%
20	4934926	Q	Resistenza 8,2 KΩ 0,5 W 2%
21	0842650	A	Dissipatore con diodi
22	0001710	A	Diodo SCR 2N683
23	0001375	Y	Diodo IN 1200 A
24	0842780	B	Dissipatore con diodi
25	0842781	A	Dissipatore con diodi
26	0818247	N	Dissipatore tipo F
27	0818242	R	Dissipatore tipo E
28	0818243	M	Dissipatore tipo D
*29	0620114	J	Piastrina SEPA
*30	0620239	K	Piastrina PIPA-A
31	0838137	M	Distanziatore
32	0001403	W	Morsettiera K 705/A
33	0839266	J	Barretta di fissaggio
34	0839352	Y	Molletta TP B
35	0830388	L	Elemento FASTON
36	0839377	R	Piastrina isolante
37	0839421	M	Guida mobile
38	0839418	J	Perno superiore
39	0834662	U	Dado
40	0834663	Y	Boccola
41	0839420	L	Squadretta
42	0833359	N	Perno
43	0837214	L	Protezione
44	0838961	G	Distanziatore
45	0001238	X	Porta fusibile
46	0001258	Z	Fusibile 0,5 A 250 V
	0001254	Y	Fusibile 12 A 250 V
	0001265	V	Fusibile 6 A 250 V

***Nota** : Per i componenti delle piastrine consultare la documentazione di ALI 130 B al Vol. 7

***Note** : For PWB component details, refer to the ALI 130 B documentation Vol. 7



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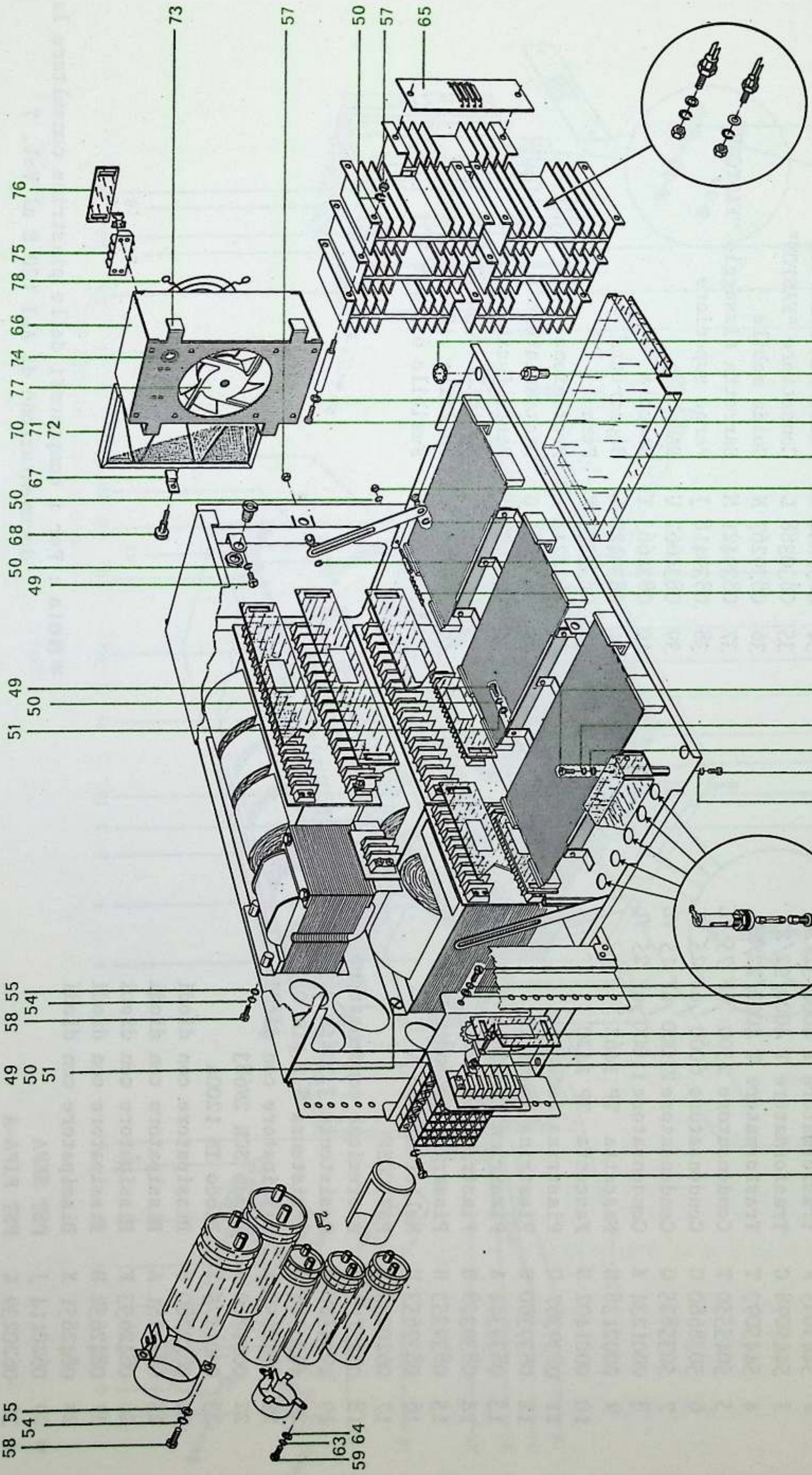
47	0834661	Q	Pulsante
48	0834665	R	Staffa
49	6311231	R	Vite TC 3 x 8
50	6332103	N	Rondella elastica ø 3,2
51	6331103	A	Rondella piana ø 3,2
52	6337106	Q	Anello elastico
53	6311245	K	Vite 4 x 15
54	6332104	B	Rondella elastica ø 4,3
55	6331104	X	Rondella piana ø 4,3
56	6311234	N	Vite TC 3 x 15
57	6321103	H	Dado M3
58	6311242	W	Vite TC 4 x 8
59	6331105	T	Rondella piana ø 5,3
60	0001858	W	Listello passacavo
61	0836945	N	Protezione PST PIPA-A
62	0836821	R	Protezione PST SEPA
63	6311258	R	Vite TC 5 x 15
64	6332105	S	Rondella elastica ø 5,3
* 65	0620104	V	PST DIAD
-	0818241	D	AG Box ventilatore
66	0819299	Q	Telaio ventilatore
67	0819293	W	Blocco filtro
68	0819150	F	Vite speciale
69	6311230	Q	Vite TC 3 x 6
-	3361200	Z	AP Filtro
70	0819304	Q	Molla
71	0819303	T	Panno per filtro
72	0819307	U	Telaio filtro
-	0818240	C	AP Supp. ventilatore
73	0819300	J	Supp. ventilatore
74	0001876	F	Passacavo
75	5612453	M	Morsettiera
76	0839336	R	Piastrina isolante
77	0001614	C	Ventilatore
78	5541340	N	Griglia ventilatore
79	0819342	P	Piastrina numerata

*Nota : Per i componenti delle piastrine consultare la documentazione di ALI 130 B al Vol. 7

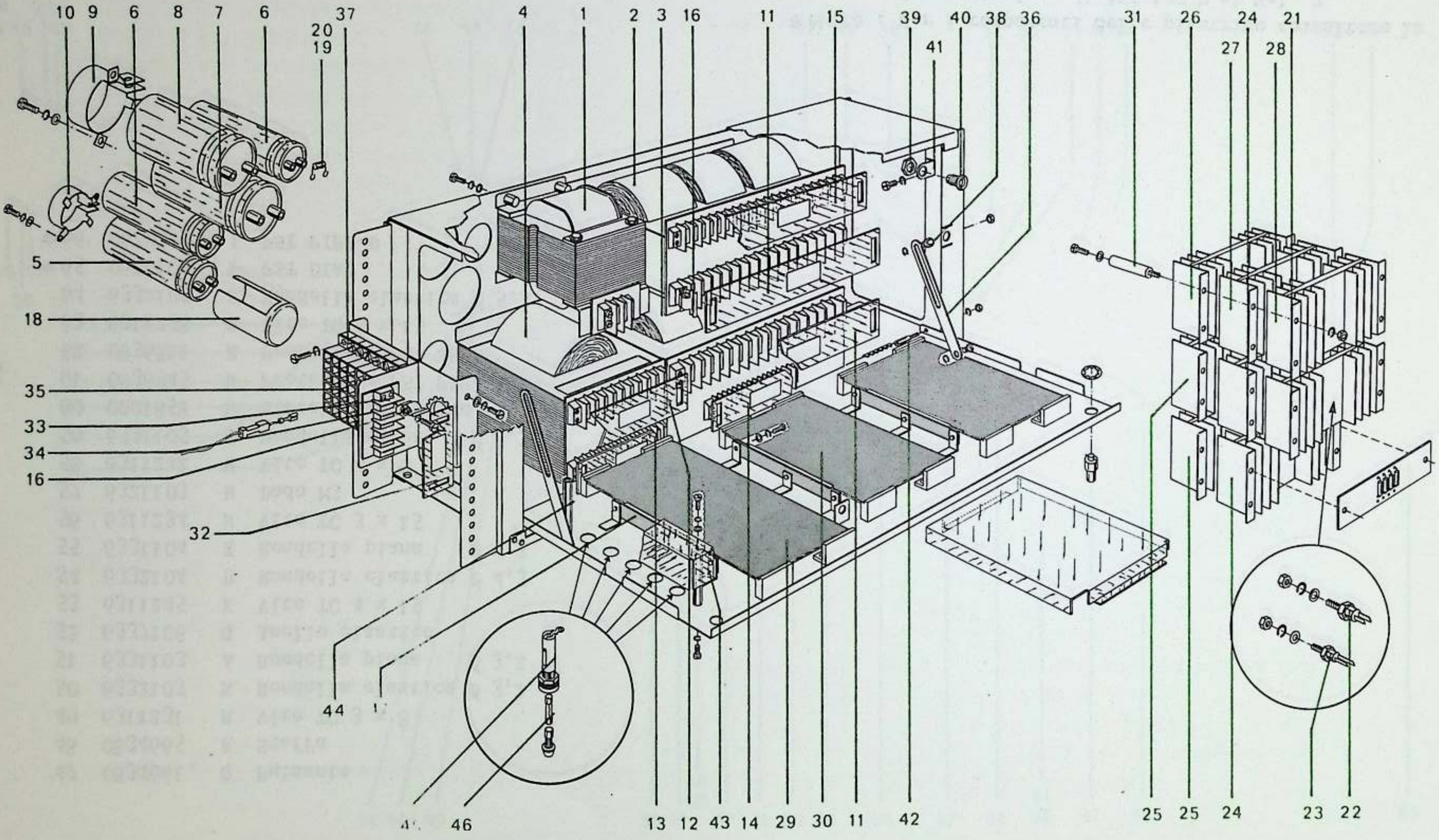
*Note : For PWB component details, refer to the ALI 130 B documentation Vol. 7



1	5421007	P	Induttanza 10 mH 6,5 A
2	5445095	F	Trasformatore T 4000/32/26
3	5445098	C	Trasformatore T 4000/32/27
4	5445093	T	Trasformatore T 4000/22/20
5	5045550	T	Condensatore 2500 /uF 75 VL
6	5038680	C	Condensatore 6000 /uF 25 VL
7	5035825	Q	Condensatore 21000 /uF 15 VL
8	0001234	X	Condensatore 11000 /uF 25 VL
9	0002138	H	Fascetta TP 1462
10	0001402	S	Fascetta TP 1420
11	0839367	Q	Piastrina isolante
12	0839360	E	Piastrina isolante
13	0839344	A	Piastrina isolante
14	0839348	B	Piastrina isolante
15	0839353	N	Piastrina isolante
16	0839653	U	Molletta tipo A
17	0620233	Z	PST COSE
18	0837218	M	Protezione condensatore
19	4934527	T	Resistenza 3,3 KΩ 0,5 W 2 %
20	4934926	Q	Resistenza 8,2 KΩ 0,5 W 2 %
21	0842650	A	Dissipatore con diodi
22	0001710	A	Diodo SCR 2N683
23	0001375	Y	Diodo IN 1200A
24	0842780	B	Dissipatore con diodi
25	0842781	A	Dissipatore con diodi
26	0842653	F	Dissipatore con dioci
27	0842652	B	Dissipatore con diodi
28	0842651	X	Dissipatore con diodi
* 29	0620114	J	PST SEFA
* 30	0620239	K	PST PIFA-A
31	0838137	M	Distanziatore
32	0839356	K	Piastrina isolante
33	5612540	D	Morsettiera K 605/A
34	0837644	X	Piastrina numerata
35	0830388	L	Connettore "FASTON"
36	0839267	N	Guida mobile
37	0839421	M	Barretta fissaggio "FASTON"
38	0839418	J	Perno superiore
39	0834662	U	Dado
40	0834663	Y	Boccola
41	0839420	L	Squadretta
42	0833359	N	Perno
43	0837214	L	Protezione
44	0838961	G	Distanziatore
45	0001238	X	Porta fusibile
46	0001258	Z	Fusibile 0,5 A 250 V
	0001254	Y	Fusibile 12 A 250 V
	0001265	V	Fusibile 6 A 250 V

***Nota** : Per i componenti delle piastrine consultare la documentazione di ALI 130 B al Vol. 7

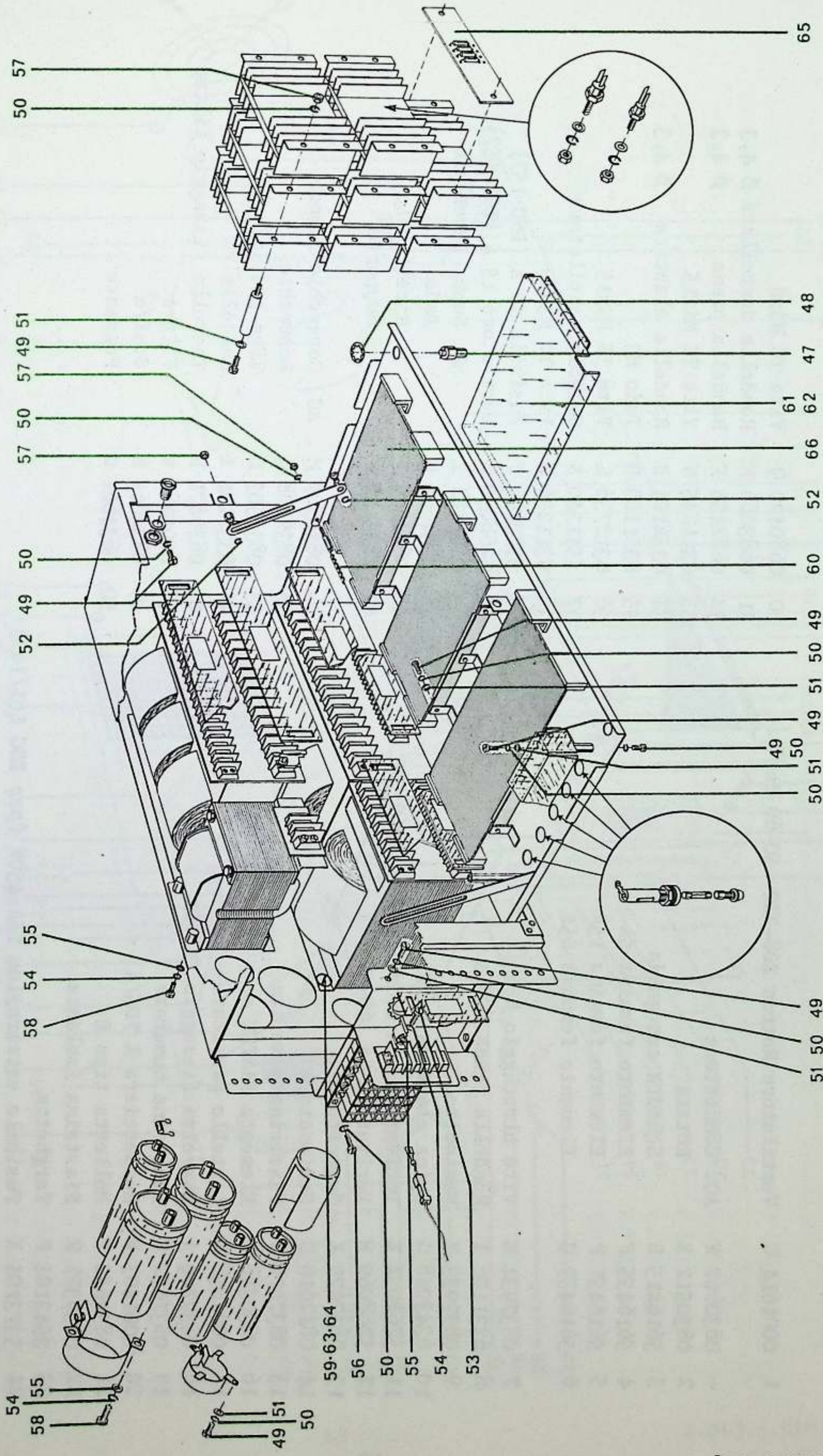
***Note** : For PWB component details, refer to the ALI 130 B documentation Vol. 7



47	0834661	Q	Pulsante
48	0834665	R	Staffa
49	6311231	R	Vite TC 3 x 8
50	6332103	N	Rondella elastica Ø 3,2
51	6331103	A	Rondella piana Ø 3,2
52	6337106	Q	Anello elastico
53	6311245	K	Vite TC 4 x 15
54	6332104	B	Rondella elastica Ø 4,3
55	6331104	X	Rondella piana Ø 4,3
56	6311234	N	Vite TC 3 x 15
57	6321103	H	Dado M3
58	6311242	W	Vite TC 4 x 8
59	6331105	T	Rondella piana Ø 5,3
60	0001858	W	Listello passacavo
61	0836945	N	Protezione PST PIPA-A.D
62	0836821	R	Protezione PST SEPA
63	6311258	R	Vite TC 5 x 15
64	6332105	S	Rondella elastica Ø 5,3
*65	0620104	V	PST DIAD
*66	0620229	J	PST PIPA-D

*Nota : Per i componenti delle piastrine consultare la documentazione di ALI 130 B al Vol. 7

*Note : For PWB component details, refer to the ALI 130 B documentation Vol. 7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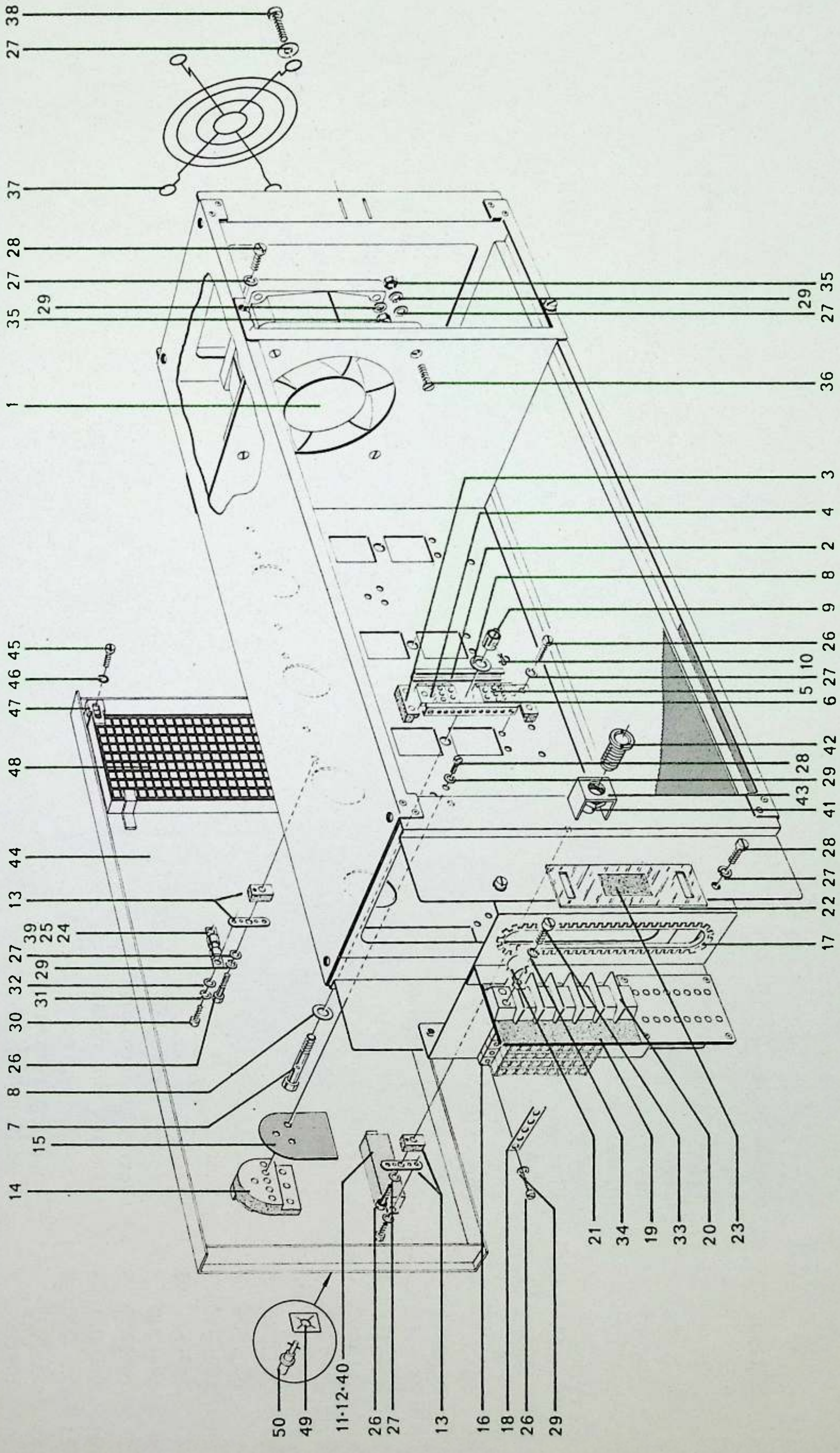
1	0001614	C	Ventilatore Rotron 208-220 50-60 Hz
-	0830662	W	AG. Connettore
2	0830512	X	Rotaia
3	5616415	B	Squadra con guida
4	5616455	F	Elemento femmina 5A
5	5616457	P	Elemento femmina 15A
6	5616459	G	Elemento femmina 25A
7	0837934	M	Vite bloccaggio box
8	6331108	Y	Rondella piana ø 8,4
9	0837933	Y	Manicotto
10	6343048	G	Spina elastica 2x12
11	5268052	Z	Derivatore 10A 60 mV (DSC 161/162)
12	5268060	M	Derivatore 2A 60 mV
13	0837679	K	Supporto
14	0842616	G	Sezionatore
15	0837678	T	Piastrina numerata
16	0830388	L	Elemento FASTON
17	0001858	W	Listello passacavo
18	0839266	J	Barretta fissaggio FASTON
19	0837652	F	Piastrina numerata
20	0001403	W	Morsettiera K 705/A
21	0839652	Y	Molletta tipo B
22	0839377	R	Piastrina isolante
23	3543104	P	Targhetta
24	5373104	X	Fusibile extrarapido 15A 450V (per DSC 161/162)
25	5373100	Z	Fusibile extrarapido 5A 450V
26	6311234	N	Vite TC M3x15
27	6331103	A	Rondella piana ø 3,2
28	6311231	R	Vite TC M3x8
29	6332103	N	Rondella elastica ø 3,2

30	0680490	Q	Vite TC M4x6
31	0683086	F	Rondella dentellata ø 4,3
32	0682456	X	Rondella piana ø 4,3
33	6311245	K	Vite TC M4x15
34	6332104	B	Rondella elastica ø 4,3
35	6321103	H	Dado M3
36	6312736	L	Vite TS M3x15
37	5541340	N	Griglia ventilatore
38	6311236	W	Vite TC M3x20
39	5373106	F	Fusibile 20 A (DSC 157)
40	5268050	L	Derivatore 15 A (DSC 157)
-	0835484	X	AP. Supp. coperchio
41	0834662	U	Dado
42	0834663	Y	Ricettacolo
43	0835132	K	Supporto
-	0836507	M	AG. Coperchio 1 mod.
44	0836508	A	Coperchio
45	0836503	L	Vite speciale
46	6331104	X	Rondella
47	0836871	N	Tassello fissaggio filtro
48	0001482	W	Filtro
49	0834665	R	Staffa
50	0834661	Q	Pulsante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39 25 24
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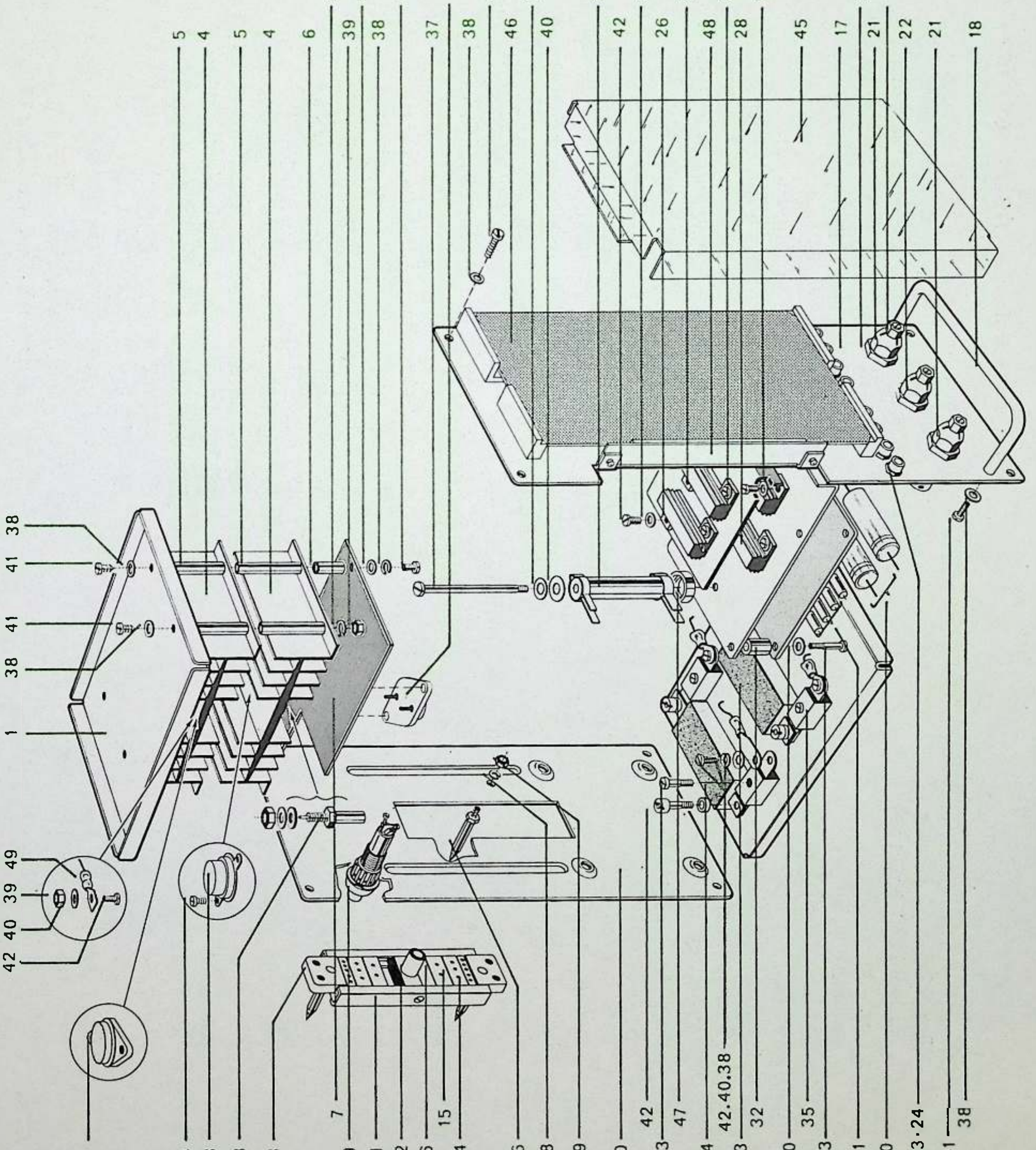
18 26

-	0842632	H	AG. Box ± 3V
1	0837937	Z	Testata
2	5836002	R	Transistore 2N3713
3	5241302	W	Termointerruttore
4	0837927	J	Dissipatore
5	0838137	M	Distanziatore
6	0838276	P	Distanziatore
7	0837657	C	Dissipatore
8	5826515	T	Diodo Zener ZL22
9	5141133	J	Pulsante RAFI
10	0837952	W	Pannello posteriore
11	0837919	Q	Rotaia Souriau
12	5616418	G	Estrattore femmina
13	5616413	J	Squadra con guida maschio
14	5616450	D	Elemento maschio 5A
15	5616452	J	Elemento maschio 15A
16	5616454	B	Elemento maschio 25A
17	0842626	K	Frontale
18	0837519	X	Maniglia
19	4999530	V	Dado
20	4999550	X	Boccola
21	4991248	M	Potenziometro 100 Ω 2W
22	4991270	R	Potenziometro 200 Ω
23	5610021	W	Boccola pup rossa
24	5610024	T	Boccola pup nera
25	0837659	U	Supporto resistenze
26	4971060	K	Resistenza 0,75 Ω 50W 3%
27	4974076	X	Resistenza 1KΩ 15W 10%
28	4971065	M	Resistenza 1Ω 50W 3%
29	4970085	W	Resistenza 0,1Ω 10W 3%
* -	0620112	Z	AP. Piastrina SEGA
30	5032090	G	Condensatore 10CC /uF
31	0001434	A	Diodi P100
32	0838682	F	Distanziatore
33	5268012	Y	Derivatore 5A 60mV
34	5268016	W	Derivatore 10A 60mV
35	0837679	K	Supporto derivatori
36	0837931	Q	Spina
37	6313113	D	Vite TC M3 x 55
38	6332103	N	Rondella elastica Ø 3,2
39	6321103	H	Dado 3MA
40	6331103	A	Rondella piana Ø 3,2
41	6311203	Q	Vite TC M3 x6
42	6311931	B	Vite TC M3 X8
43	6311234	N	Vite TC M3 x15
44	0680116	G	Vite TC 2,6 MA x8
45	0836820	Q	Protezione PST AMER
*46	0620115	N	PST. AMER
47	0001506	Y	Supporto SECI
48	0620116	S	PST. COAM

***Nota** : Per i componenti delle piastrine consultare la documentazione di ALI 130 B al Vol. 7

***Note** : For PWB component details, refer to the ALI 130 B documentation Vol. 7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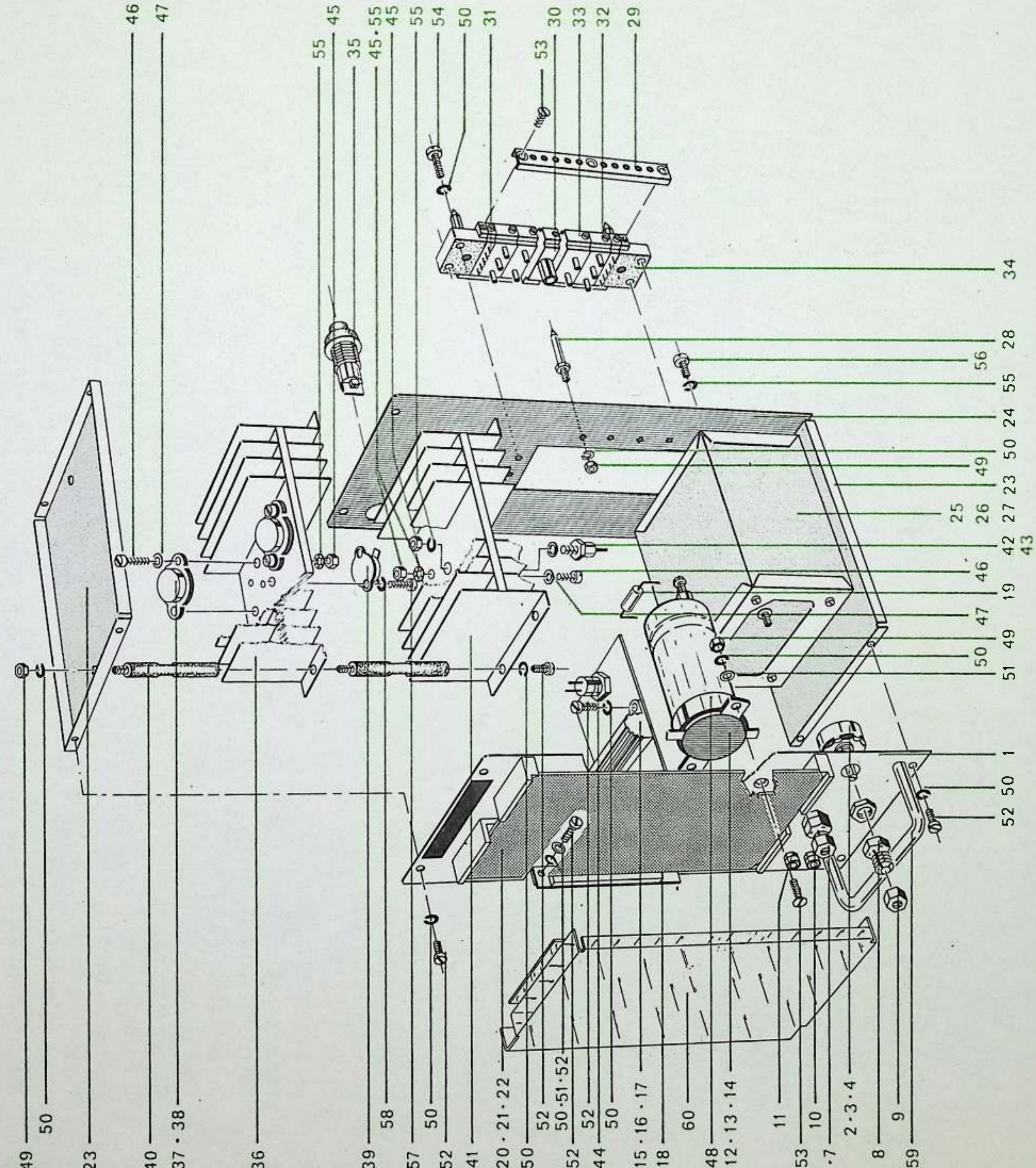
–	0842532	F	AG. Box +5
–	0842634	S	AG. Box +6 (DSC 161/162)
–	0842635	W	AG. Box –36
1	0842893	G	Frontale
2	4993540	C	Potenz. 10 KΩ 4W (Box –36)
3	4991070	W	Potenz. 5 KΩ 2W (Box +6) (DSC 161/162)
4	4991070	W	Potenz. 5 KΩ 2W (Box +5)
5	4993305	A	Potenz. 330 Ω 2W (Box +5)
6	4993305	A	Potenz. 330 Ω 2W (Box +6) (DSC 161/162)
7	4991415	Z	Potenz. 2,5 KΩ 2W (Box –36)
8	4999550	X	Boccola bloccaggio potenz.
9	4999530	V	Dado bloccaggio potenz.
10	5610021	W	Boccola pup nera
11	5610024	J	Boccola pup rossa
12	0001307	L	Cond. 1000 /uF 40V (Box –36)
13	5035679	S	Cond. 6400 /uF 15V (Box +6) (DSC 161/162)
14	5035679	S	Cond. 6400 /uF 15V (Box +5)
15	4973474	Z	Resist. 270Ω 50W 3% (Box –36)
16	4971086	B	Resist. 2,5Ω 50W 3% (Box +6) (DSC 161/162)
17	4971086	B	Resist. 2,5Ω 50W 3% (Box +5)
18	0620234	N	Piastrina con connettore
19	5041355	Q	Condensatore 6,8 /uF 35V (Box +5, +6)
	5041455	S	Condensatore 22 /uF 50V (Box –36)
*20	0620243	S	PST CIBO–A per Box +5V
*21	0620231	R	PST CIBO–E per Box +6 (DSC 161/162)
*22	0620240	R	PST CIBO–D per Box –36
23	0837937	Z	Testata
24	0837956	X	Pannello posteriore
25	5421004	B	Induttanza 10 mH 5A (Box –36)
26	5421000	E	Induttanza 1 mH 15A (Box +6) (DSC 161/162)
27	5421000	E	Induttanza 1 mH 15A (Box +5)
28	0837931	Q	Spina
29	0830512	X	Rotaia Souriau
30	5616418	G	Estrattore femmina
31	5616450	T	Elemento maschio 5A
32	5616452	J	Elemento maschio 15A
33	5616454	B	Elemento maschio 25A
34	5616413	J	Squadra con guida
35	5141133	N	Pulsante RAFI
36	0837927	J	Dissipatore
37	5836002	B	Transistor 2N3713
38	5836000	C	Transistor 2N3772
39	5241302	W	Termostato Klixon
40	0838137	M	Distanziale
41	0837928	M	Dissipatore
42	5812010	W	Diodo 1N 1200A (Box –36)
43	5812012	B	Diodo contr. 1N3899 (Box +5, +6)
44	0001710	A	Diodo controllato 2N 683
45	0682260	E	Dado M4
46	0680550	G	Vite TC M4x15
47	0682456	X	Rondella piana ø 4,2
48	0001402	S	Fascetta condensatore
49	6321103	H	Dado M3
50	6332103	N	Rondella elastica ø 3,2
51	6331103	A	Rondella piana ø 3,2
52	6311230	Q	Vite TC M3x6
53	6312732	K	Vite TS M3x6
54	6311233	Z	Vite TC M3x12
55	6332104	B	Rondella elastica ø 4,2
56	6311243	S	Vite TC M4x10
57	0680116	C	Vite TC M2,6x8
58	0683040	M	Rondella elastica ø 2,8
59	0837519	E	Maniglia
60	0837160	R	Protezione piastrine

* Nota : Per i componenti delle piastrine consultare la documentazione di ALI 130 B al Vol. 7

* Note : For PWB component details, refer to the ALI 130 B documentation Vol. 7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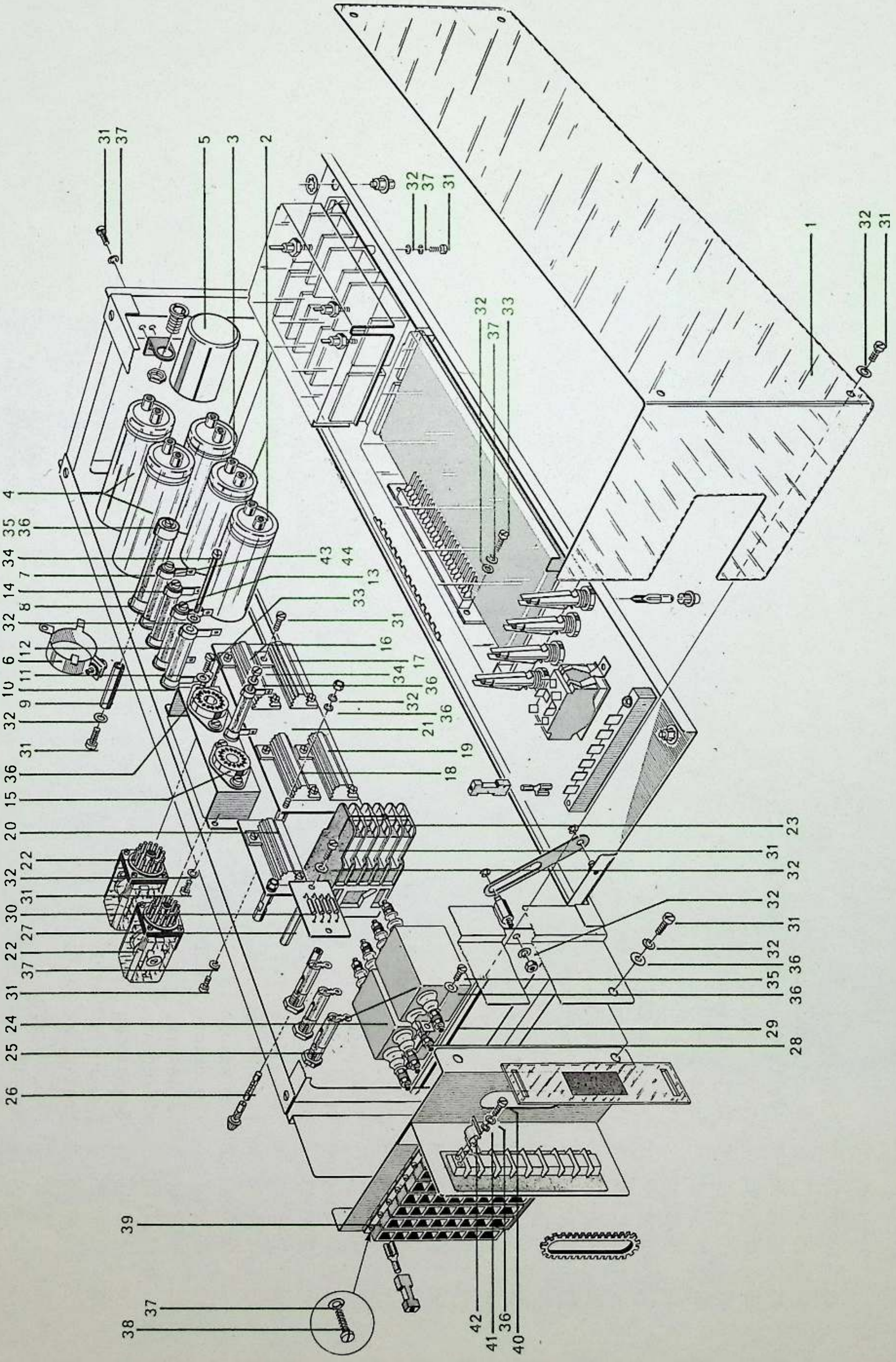
1	0837630	Y	Protezione
2	0001309	D	Condensatore 500 uF 100VL
3	0002125	B	Condensatore 3200 uF 40VL
4	5045270	P	Condensatore 1100 uF 75VL
5	0837218	M	Protezione condensatori
6	0001402	S	Fascetta TP 1420
7	4973077	E	Resistenza 100 Ω 25W
8	0002118	F	Supporto TP ID13
9	0837633	H	Distanziatore
10	0001506	V	Supporto TP ID10
11	4973633	C	Resistenza 390 Ω 15W
12	4973600	C	Resistenza 330 Ω 15W
13	4973230	K	Resistenza 150 Ω 15W
14	4972832	Z	Resistenza 62 Ω 25W
15	0001370	W	Zoccolo Undecal
16	4973761	Z	Resistenza 560 Ω 50W
17	4973235	M	Resistenza 150 Ω 50W
18	4973636	H	Resistenza 390 Ω 50W
19	4973450	Z	Resistenza 220 Ω 50W
* 20	4973798	A	Resistenza 5,1 Ω 50W
21	0836825	J	Piastrina
22	0001386	H	Relè 3PDT 12 VCC
* 23	5326600	B	Teleruttore
24	5427065	A	Filtro FL100-139 ICAR
25	0001238	X	Portafusibile LITTELFUSE
26	0001254	Y	Fusibile 12A 250V
27	0838137	M	Distanziatore
28	0837380	X	Distanziatore
29	0837988	T	Distanziatore
* 30	0620111	M	Piastrina RATE
31	6311231	R	Vite TC M3 x8
32	6331103	A	Rondella piana Ø 3,2
33	6311230	Q	Vite TC M3 x6
34	6313113	D	Vite TC M3 x55
35	6311242	W	Vite TC M4 x8
36	6331104	X	Rondella piana Ø 4,3
37	6332103	N	Rondella elastica Ø 3,2
38	6311234	N	Vite TC 3M x15
39	0839264	A	Barretta fissaggio FASTON
40	6311245	K	Vite TC M4 x15
41	6332104	B	Rondella elastica Ø 4,3
42	0839653	U	Molletta tipo A
43	9940338	D	Rondella Ø 3,3
44	0839117	P	Tirante

***Nota** : Con teleruttore a rif. 23 utilizzare la resistenza a rif. 20

***Note** : For breaker, specified at Ref. 23, use resistor at Ref. 20

***Nota** : Per i componenti delle piastrine consultare la documentazione di ALI 130 B al Vol. 7

***Note** : For PWB component details, refer to the ALI 130 B documentation Vol. 7



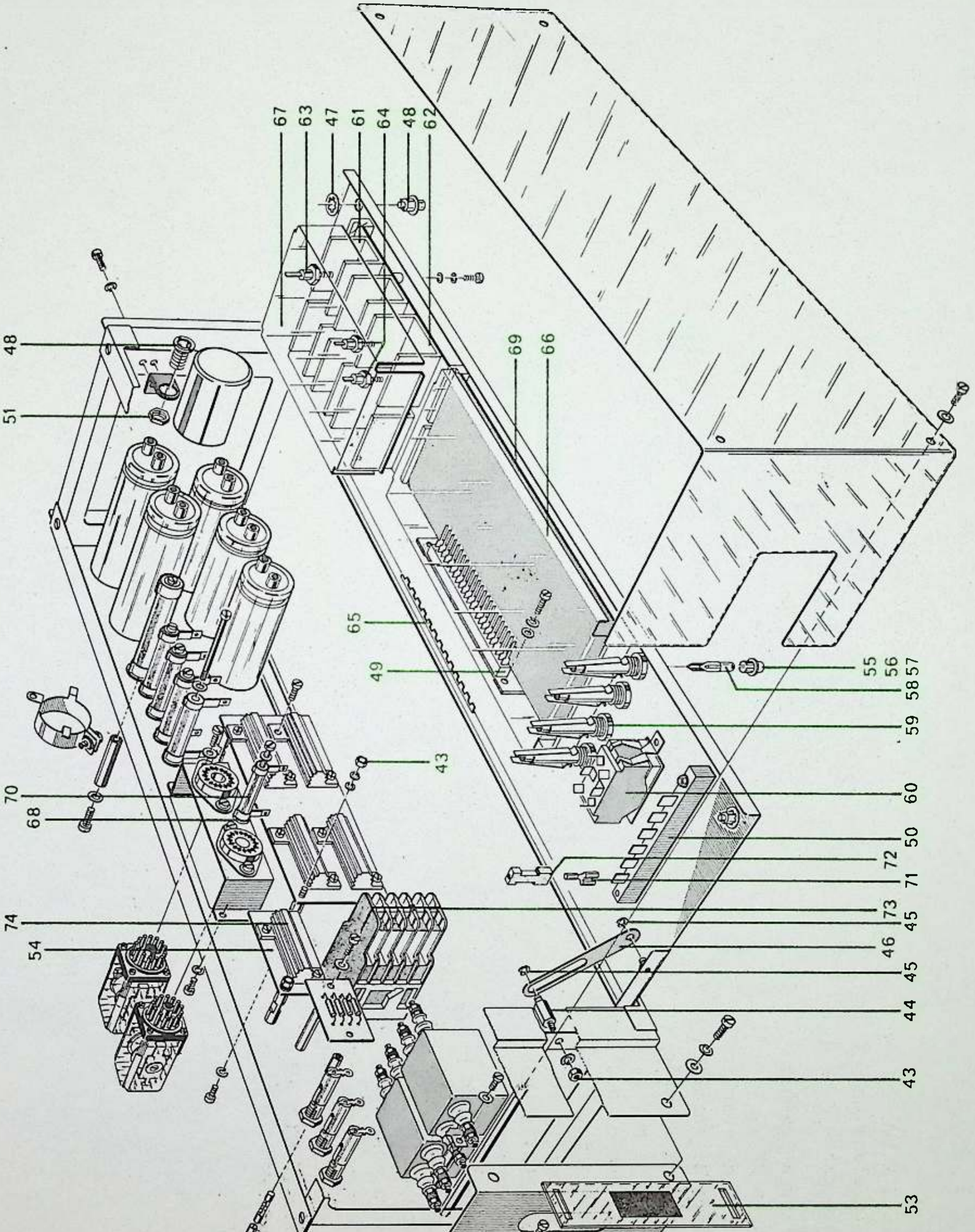
43	6321103	H	Dado M3
44	0839418	J	Perno superiore
45	6337106	Q	Anello di tenuta benzing Ø 3,5
46	0837634	W	Guida mobile
47	0834662	U	Molla di tenuta
48	0834661	Q	Pulsante
49	0620233	Z	PST COSE
50	0830388	L	Elemento FASTON
51	*0001692	J	Morsettiera K 608/A
52	0836826	M	Piastrina numerata
53	0839359	G	Piastrina isolante
54	0836824	N	Piastrina
55	5363153	S	Gemma (gialla
56	5363154	P	Gemma (verde
57	5363152	W	Gemma (rossa
58	5361011	M	Lampadina 12V
59	5363150	R	Portalampada RAFI
60	5104015	H	Deviatore
61	0837641	S	Dissipatore
62	0837318	P	Dissipatore
63	5826515	T	Diodo Zener ZL22
64	5826513	A	Diodo Zener 10Z
65	0001858	W	Listello passacavo
66	0836823	Z	Protezione PST COMA
67	0836946	S	Protezione DIODI
68	0001506	V	Isolatore
*69	0620113	V	PST.COMA
70	4972956	W	Resistenza 82 Ω 15W
71	0000883	J	Terminale FASTON
72	0830396	U	Protezione FASTON
*73	5326620	Z	Teleruttore
*74	4979005	V	Resistenza 3,9K Ω

* **Nota** : Con teleruttore a rif. 73 utilizzare la resistenza a rif. 74

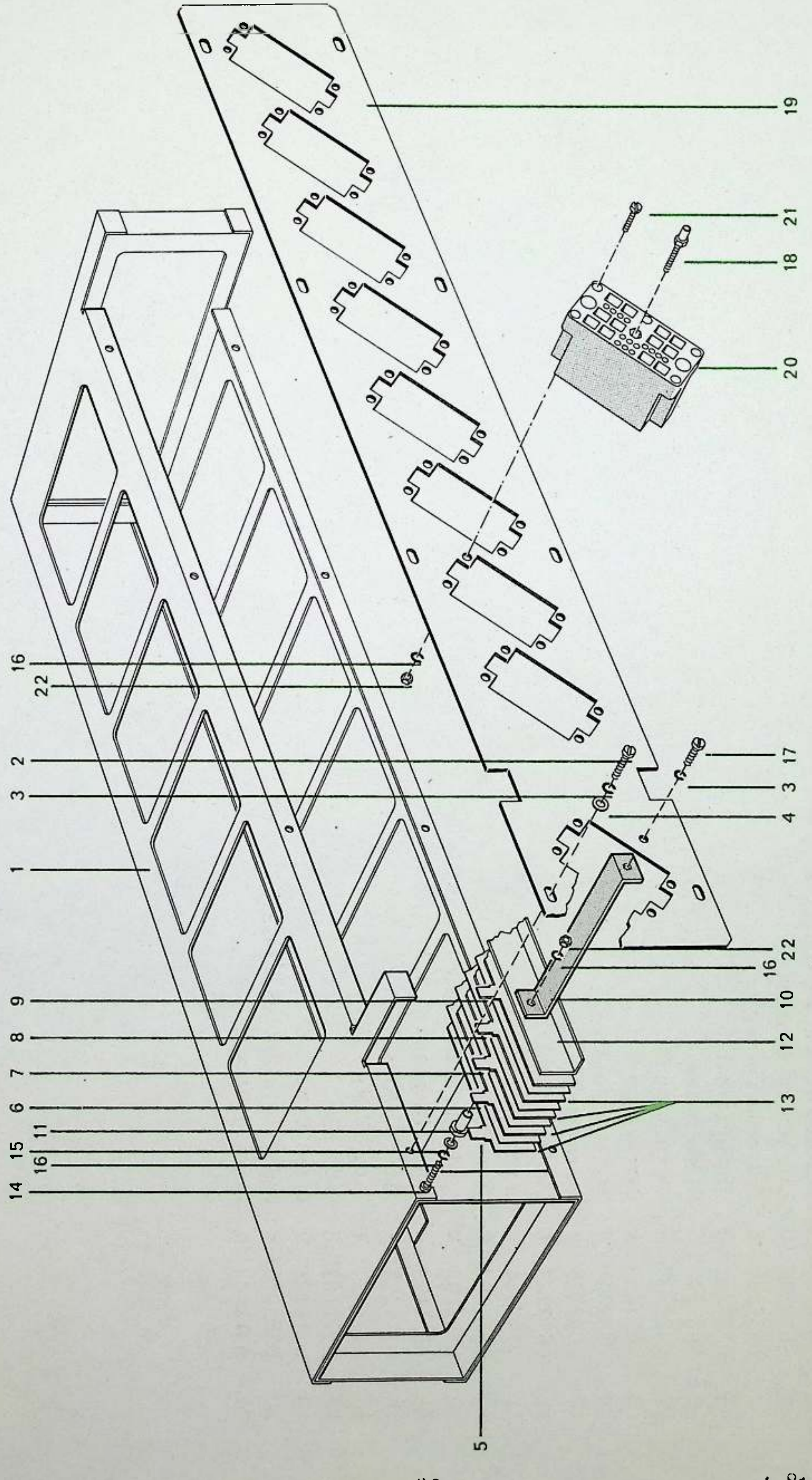
* **Note** : For breaker, specified at Ref. 73, use resistor at Ref. 74

* **Nota** : Per i componenti delle piastrine consultare la documentazione di ALI 130 B al Vol. 7

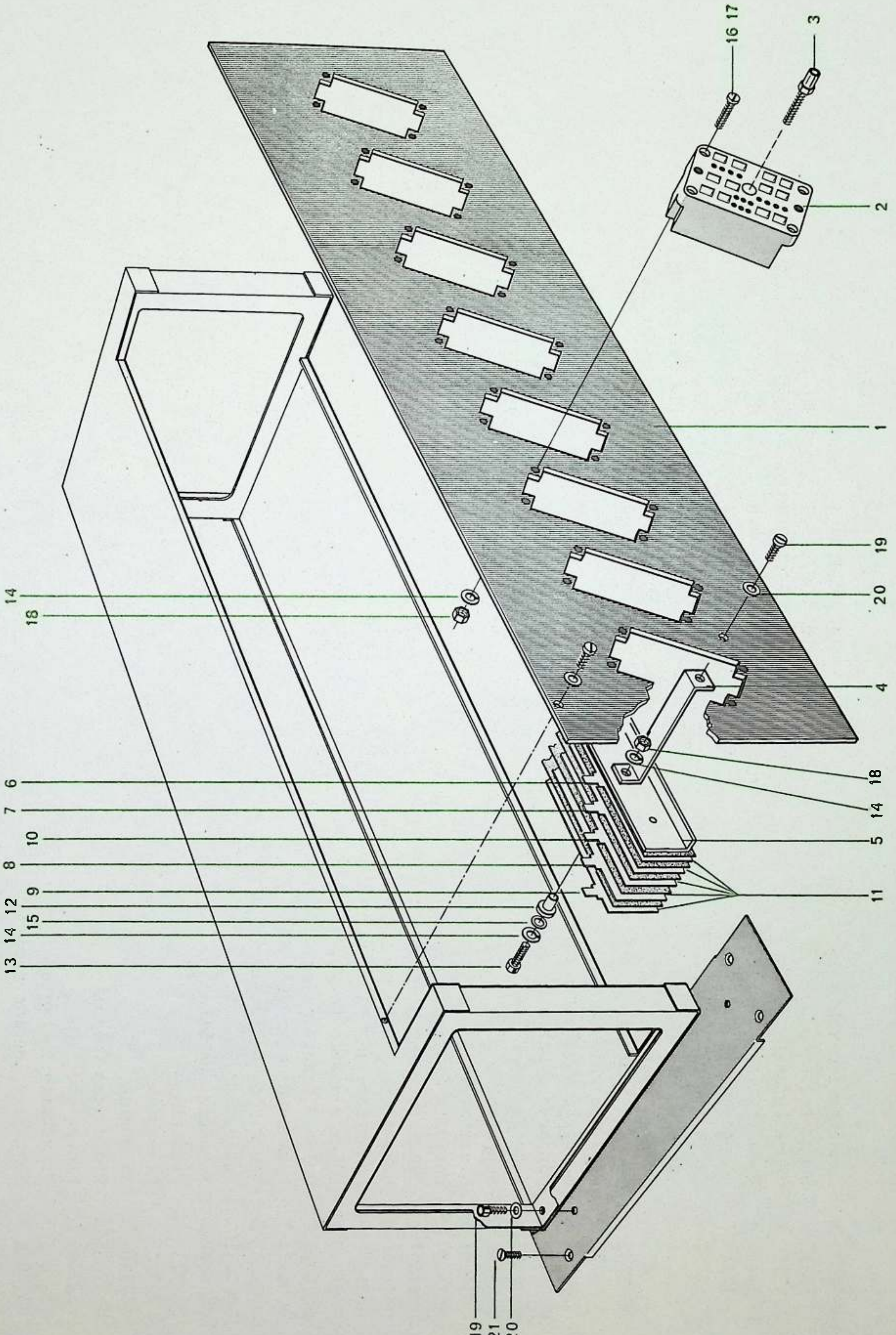
* **Note** : For PWB component details, refer to the ALI 130 B documentation Vol. 7



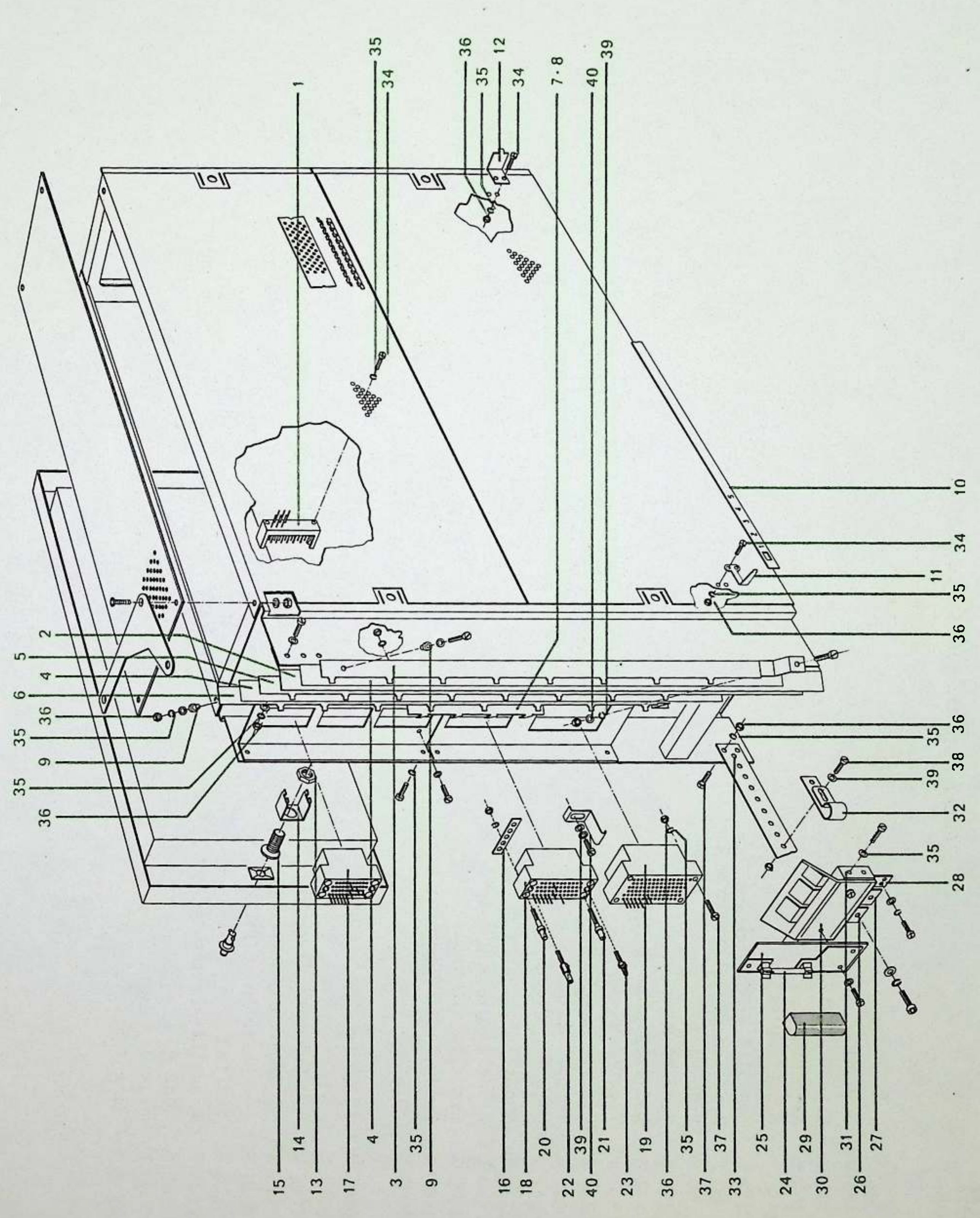
1	0819117 M	Telaio
2	6311243 S	Vite TC 4 x 10
3	6332104 B	Rondella elastica Ø 4,3
4	6331104 X	Rondella piana Ø 4,3
–	0643358 W	AG. Piastra scambio
5	0819110 B	Barra P1
6	0819112 Q	Barra di scambio
7	0819113 L	Barra di scambio
8	0819114 H	Barra di scambio
9	0819115 D	Barra di massa
10	0837246 X	Traversa di sostegno
11	0837244 P	Boccola isolante
12	0819108 M	Rinforzo barre
13	0819107 X	Bandella isolante
14	6311234 N	Vite TC M3 x 15
15	6331103 A	Rondella piana Ø 3,2
16	6332103 N	Rondella elastica Ø 3,2
17	6311242 W	Vite TC M4 x8
18	5616022 Q	Estrattore
19	0819109 R	Piastra porta connettori
20	5616020 B	Connett. AMP 29 CT
21	6311232 V	Vite TC M3 x 10
22	6321103 M	Dado M3



1	0837242	W	Piastra porta connettori
2	5616020	B	Connettore AMP 29 contatti
3	5610022	Q	Estrattore femmina
4	0837246	X	Traversa sostegno
5	0837245	K	Rinforzo barre
6	0837243	S	Barra masse
7	0837237	S	Barra tipo D
8	0837239	K	Barra tipo B
9	0837241	J	Barra tipo A
10	0837238	P	Barra tipo C
11	0837247	T	Bandella isolante
12	0837244	P	Boccola isolante
13	6311234	N	Vite TC M3 x 15
14	6332103	N	Rondella elastica Ø 3,2
15	6331103	A	Rondella piana Ø 3,2
16	6311232	V	Vite TC M3 x10
17	6311236	W	Vite TC M3 x 20
18	6321103	H	Dado M3
19	6311242	W	Vite TC M4 x 8
20	0683086	F	Rondella elastica Ø 4,3
21	6312743	Q	Vite TS M4 x 8


16 17

1	0834000	S	Connettore maschio
2	0837252	X	Supporto barre
3	0837251	K	Barra laterale destra
4	0837256	Y	Bandella isolante
5	0837249	L	Barra centrale
6	0837250	J	Barra laterale sinistra
7	0837254	Q	Barra – -3V
8	0837255	L	Isolante per -3V
9	0837753	D	Boccola isolante
10	0839772	W	Riga numerata
11	0839474	P	Supporto a balestra sinistro
12	0839473	S	Supporto a balestra destro
13	0834662	X	Dado Fastener
14	0835132	C	Supporto
15	0834663	Y	Ricettacolo
16	0838039	M	Barretta fissaggio connettore
17	0842491	F	Connettore AMP 34 contatti
18	0842490	E	Connettore AMP 50 contatti
19	0001426	R	Connettore AMP 75 contatti
20	0001700	K	Guida d'angolo femmina
21	0001699	R	Guida d'angolo maschio
22	0001124	T	Femmina di accoppiamento
23	0001123	E	Maschio di accoppiamento
24	0001231	Z	Fusibile
25	0842808	Z	Supporto fusibile
26	0837259	M	Piastrina
27	0837742	G	Piastrina
28	0837668	S	Piastrina
29	0837258	R	Protezione fusibile
30	0837257	U	Protezione
31	0837671	V	Traversino isolante
32	5618054	V	Serracavo Looping tipo 3
33	0834139	J	Bandella reggicavi
34	6307430	Q	Vite TC 3MAx6
35	6331103	N	Rondella elastica Ø 3,2
36	6321103	H	Dado M3
37	6311232	V	Vite TC M3x10
38	6311247	T	Vite TC M4x20
39	6331104	X	Rondella piana Ø 4,3
40	6332104	X	Rondella elastica Ø 4,3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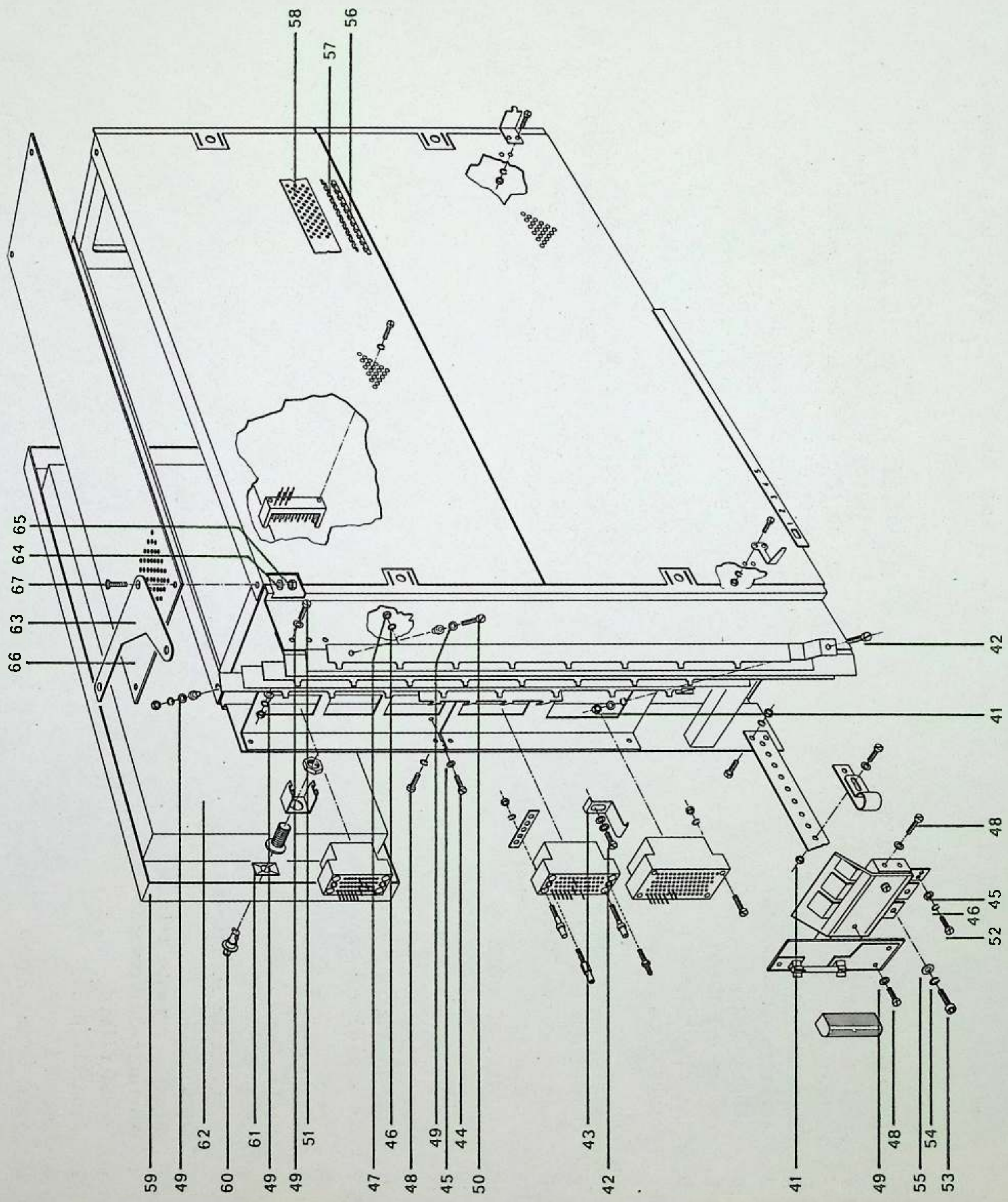
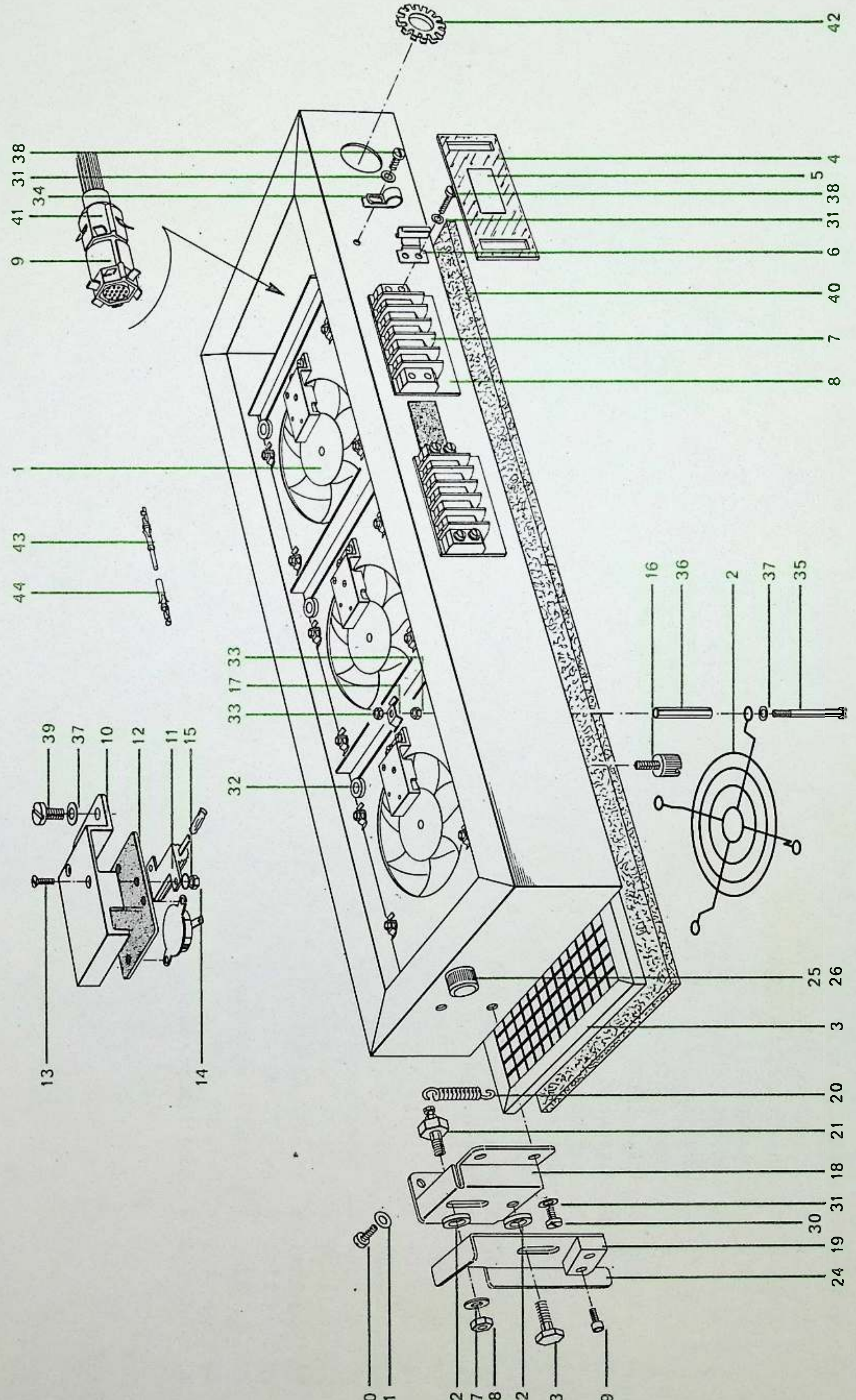
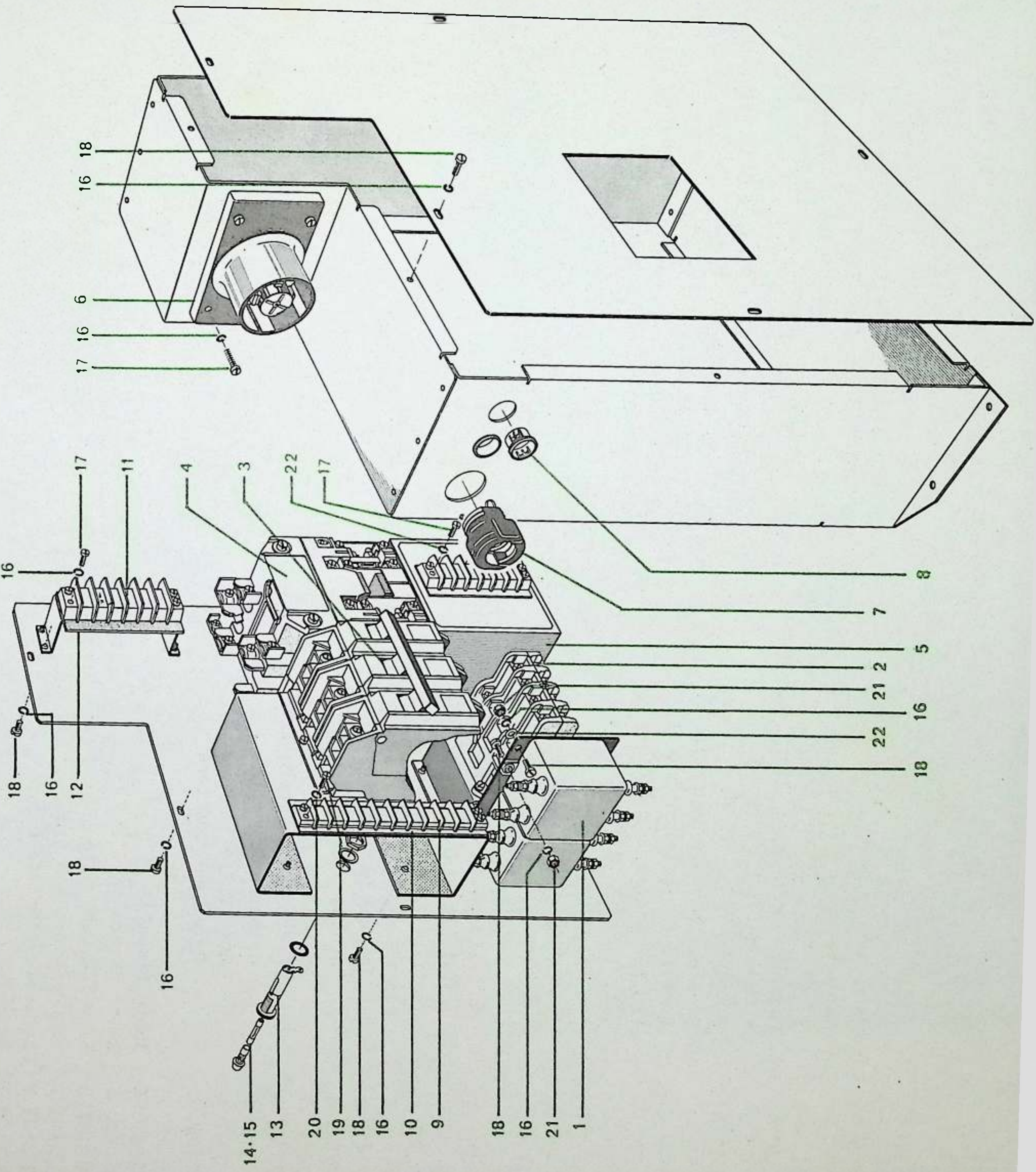
41	6321104 W	Dado M4
42	6311244 P	Vite TC M4x12
43	0837262 Y	Aggancio
44	0680550 E	Vite TC M4x15
45	0682456 X	Rondella piana ∅ 4,3
46	0683086 F	Rondella dentellata ∅ 4,3
47	0682260 E	Dado M4
48	6311231 R	Vite TC M3x8
49	6331103 A	Rondella piana ∅ 3,2
50	6311236 W	Vite TC M3x20
51	6311234 N	Vite TC M3x15
52	0680541 E	Vite TC M4x12
53	0680311 X	Vite TCE M8x15
54	0683131 E	Rondella elastica ∅ 8,4
55	0682560 L	Rondella piana ∅ 8,4
56	0834008 Z	Bandella di massa
57	0834007 C	Bandella di alimentazione
58	0834009 V	Nastro isolante
-	0836264 M	AG. Coperchio 1 MOD.
59	0836282 E	Coperchio
60	0834661 Q	Pulsante Fastener
61	0834665 R	Staffa elastica
62	0674543 B	Pannello in PVC
63	0675226 U	Staffa
64	6332105 F	Rondella elastica ∅ 5,3
65	6321105 S	Dado M5
66	0836940 L	Piastra forata
67	6313725 B	Vite T.S.C.E. 5x20



1	0001614	C	Ventilatore Boxer 208-230V 50-60 Hz
2	5541340	N	Griglia per ventilatore
3	0001481	J	Filtro
4	0839356	K	Piastrina isolante
5	3543104	P	Targhetta autoadesiva
6	0839653	U	Molletta tipo A
7	5612540	D	Morsettiera K 605
8	0000867	H	Piastrina numerata
9	5613858	Y	Connettore 12
–	0842609	G	AG. Protezione ventilatori
10	0837664	Z	Scatola protezione
11	4962961	R	Resistenza 70Ω 8W
12	0842638	T	Piastrina con termoswitch
13	6312725	F	Vite TS 2MAx8
14	0682865	D	Dado 2MA
15	0683542	T	Rondella elastica Ø 2,2
16	0674159	N	Vite fissaggio ventilatore
17	0837215	Q	Molla blocco dadi
18	0674139	L	Guida
19	0674501	B	Blocchetto
20	0674143	T	Molla
21	0674141	K	Stud
22	0674145	L	Distanziale in delrin
23	0674142	X	Stud
24	0674502	P	Piastra arresto telaio
25	0674149	M	Nottolino di comando
26	0674146	Y	Ferma Filtro
27	6331105	T	Rondella Ø 5,3
28	6321105	S	Dado M5
29	6313102	L	Vite T.C.E. M3x10
30	6311242	W	Vite T.C. M4x8
31	6332104	B	Rondella elastica Ø 4,3
32	0001876	F	Passacavo a scatto
33	6321103	H	Dado M3
34	5618052	C	Serracavo Looping tipo 1
35	7454750	B	Vite M3x50
36	0838723	X	Distanziatore
37	6331103	A	Rondella piana Ø 3,2
38	6311247	J	Vite T.C. M4x15
39	6311231	R	Vite T.C. M3x8
40	0836848	R	Panno per filtro
41	5613860	S	Connettore femmina 12 CT
42	0001858	W	Listello passacavo
43	0000885	B	PIN amp. maschio
44	0000887	K	PIN amp. femmina


31 38
25 26
31 38

1	0001449	G	Filtro RF ICAR
2	0001822	H	Contattore 24V 60 Hz
	0001821	V	Contattore 24V 50 Hz
3	0001355	W	Breaker
4	0001885	C	Contattore 24V 50 Hz
	0001884	G	Contattore 24V 60 Hz
5	0001315	S	Trasformatore TP 40000.22.8
6	0001354	S	Spina INLET
7	0001373	F	Passacavo
8	0001875	T	Passacavo a scatto
9	5612595	K	Morsettiera K 511/A
10	0837277	W	Piastrina numerata
11	5612447	M	Morsettiera K 606/A
12	0837275	N	Piastrina numerata
13	0001238	X	Porta fusibile
14	0001218	Y	Fusibile 0,5 A
15	0001244	X	Fusibile 3A
16	6332304	F	Rondella elastica Ø 4,3
17	6311245	K	Vite TC M4 x 15
18	6311243	S	Vite TC M4 x 10
19	6311234	N	Vite TC M3 x 15
20	6332303	J	Rondella elastica Ø 3,2
21	6321104	W	Dado M4
22	6331104	X	Rondella piana Ø 4,3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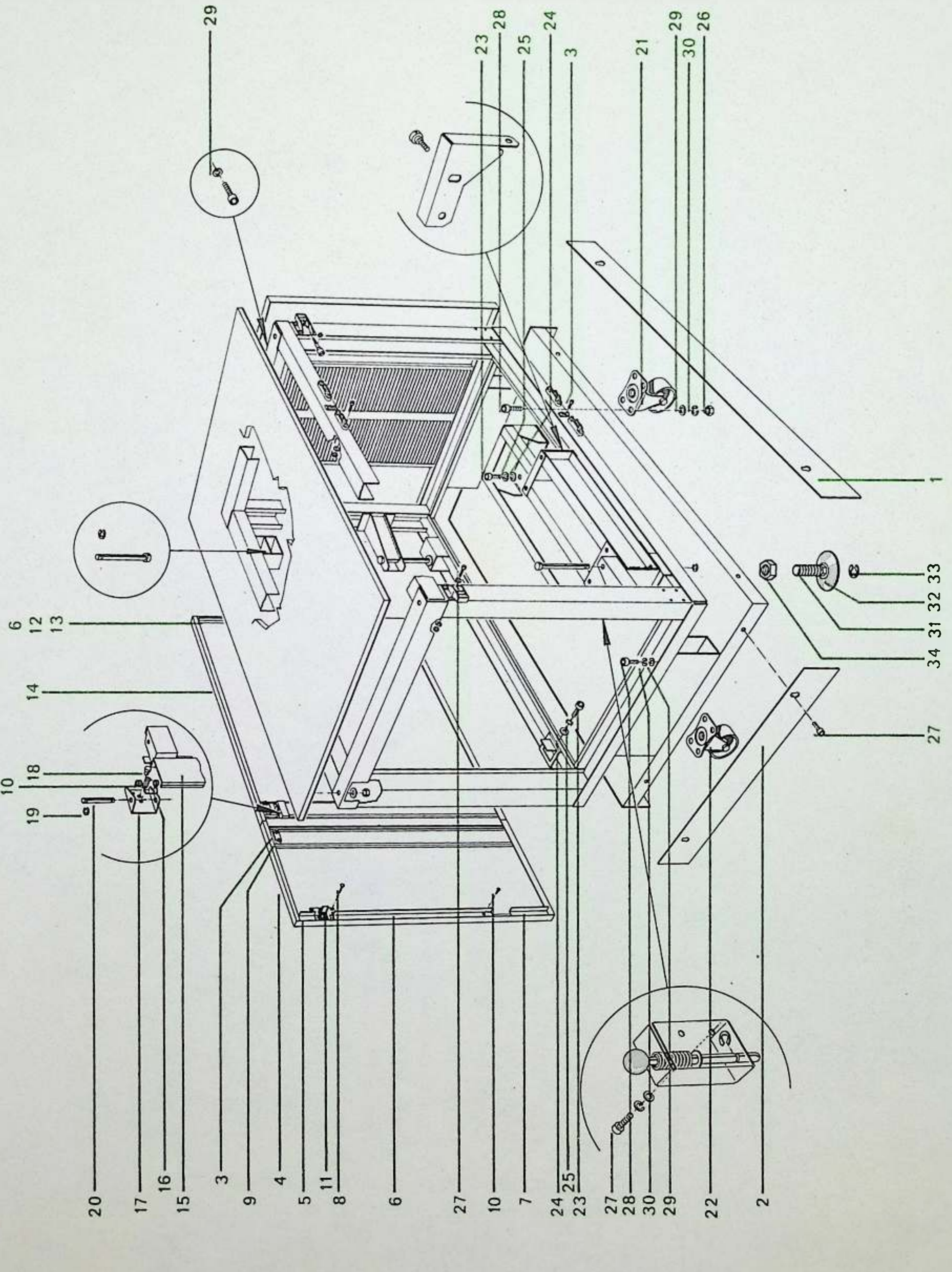
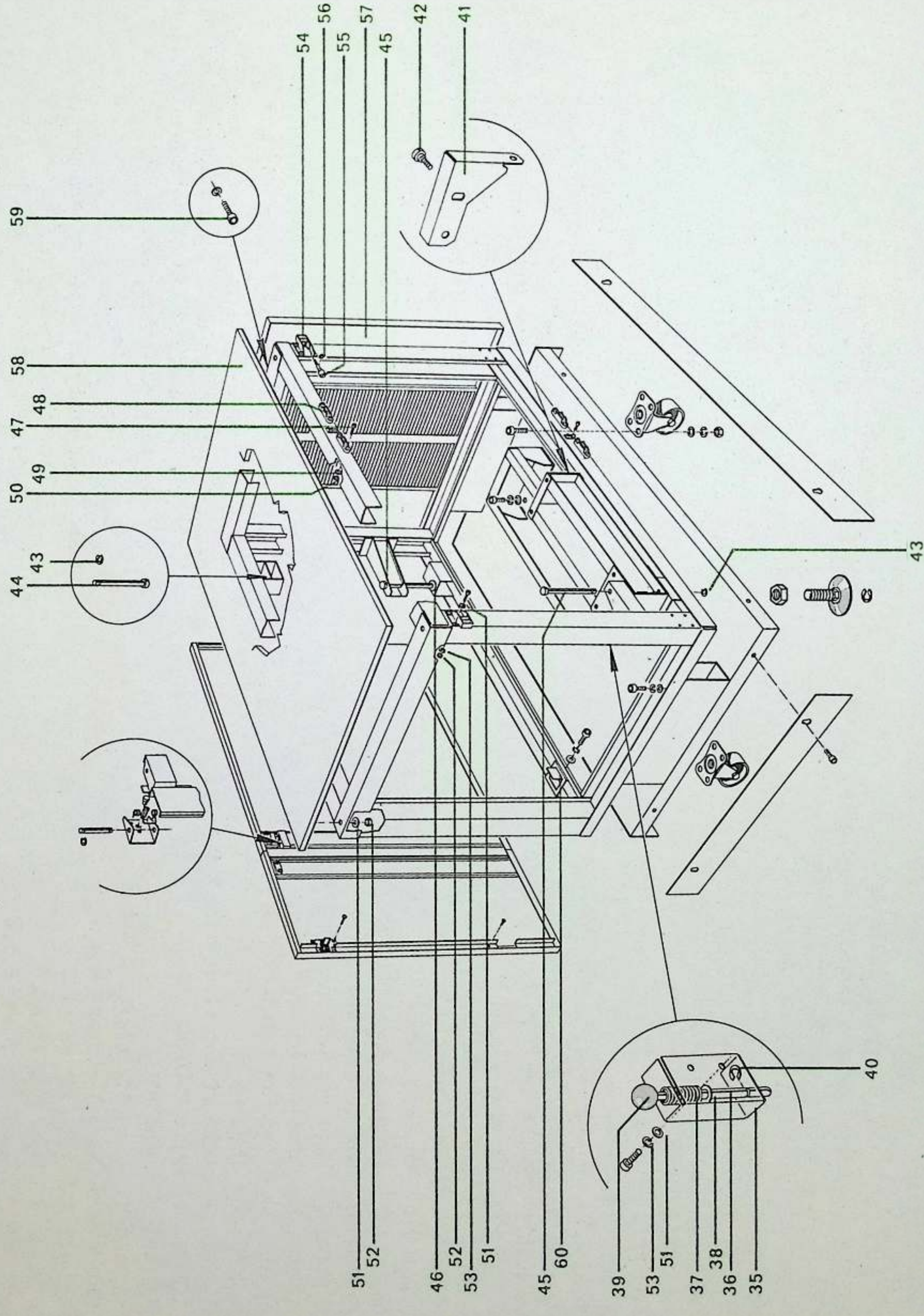
1	0674965	N	Copertura ant. e post.
2	0674953	V	Copertura laterale
-	0676540	A	AG. Pannello post. sin. - ant. destro
3	6348324	G	Vite autof.T.S. a croce
4	0675318	N	Pannello
5	0676529	B	Profilo laterale superiore
6	0676528	F	Profilo laterale centrale
7	0676526	N	Profilo laterale inferiore
8	6313710	G	Vite T.S.C.E. 4x10
9	0005331	U	Piastrina per magnete
10	6348290	X	Vite autof. T.C. cava a croce
11	0675266	Y	Cerniera
-	0676539	C	AG. Pannello post. destro - ant. sinistro
12	0676530	H	Profilo laterale superiore
13	0676527	J	Profilo laterale inferiore
14	0675323	Z	Pannello
-	0676535	B	AP. Antina ribaltabile
15	0676522	M	Gruppo profilo
16	0674048	Y	Molla
17	0675327	S	Parte esterna cerniera
18	0005338	S	Gommino paracolpi
19	6337106	Q	Anello elastico
20	0674050	S	Perno per cerniera
21	6476416	X	Ruota fissa
22	6476420	S	Ruota pivotata
23	6313132	B	Vite T.C.C.E. 5x15
24	6331105	T	Rondella piana ø 5,3
25	6332105	F	Rondella elastica ø 5,3
26	6321106	E	Dado M6
27	6313116	A	Vite T.C.C.E. 4x12
28	6313148	W	Vite T.C.C.E. 6x15
29	6331106	F	Rondella piana ø 6,4
30	6332106	K	Rondella elastica ø 6,4
-	0674593	Q	AG. Piedino di livellamento
31	0674943	U	Vite piede
32	0674944	R	Piede
33	6337120	Y	Anello di tenuta
34	6321120	N	Dado M20



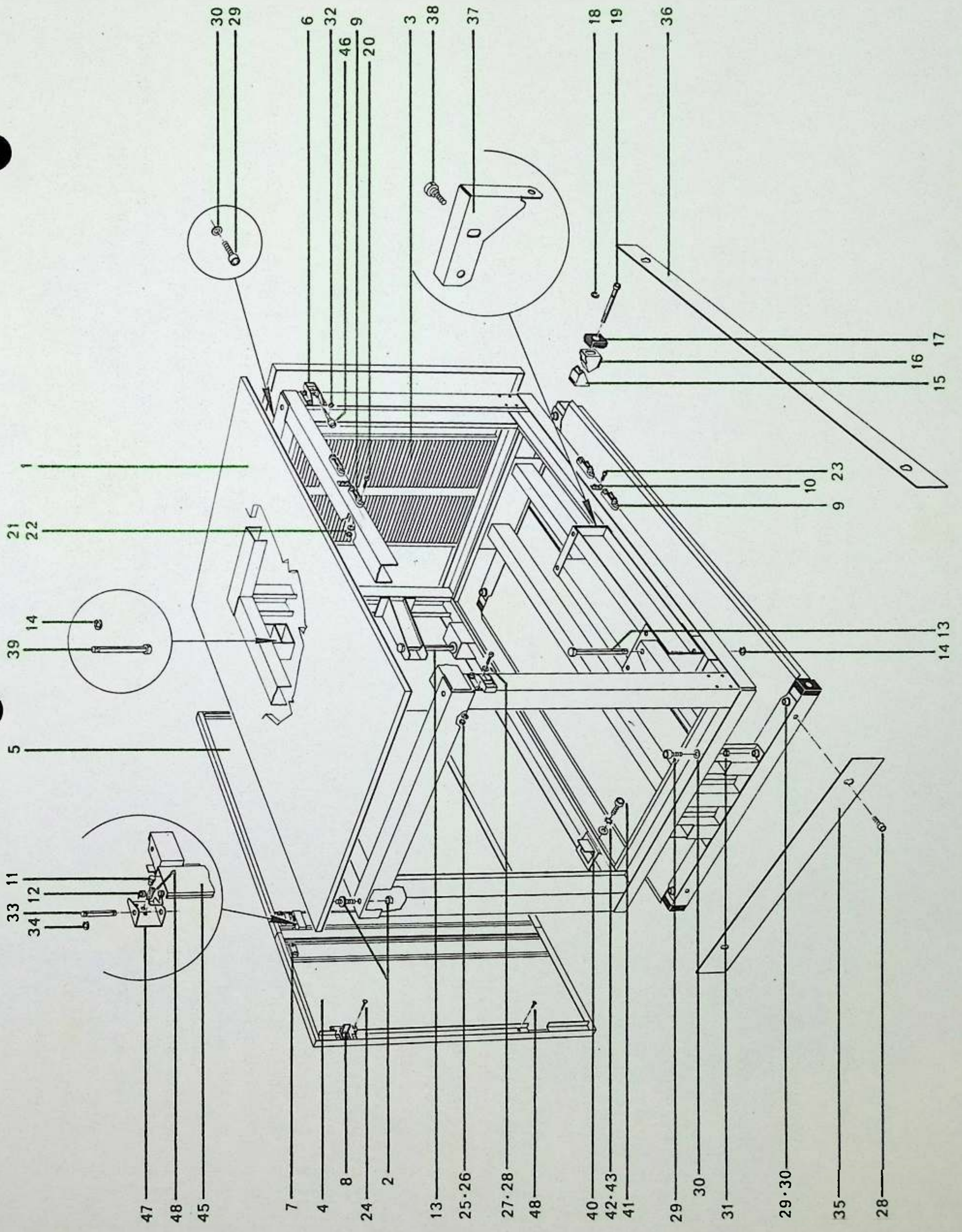
-	0676295	B	AG. Dispositivo di sicurezza
35	0676296	P	Canotto
36	0676292	N	Albero
37	0676294	F	Molla
38	0676291	A	Rondella
39	6371522	G	Pomello
40	6337112	C	Anello Benzing
41	0677018	H	Gancio di arresto
42	0677257	B	Vite di perno
43	6337114	V	Anello Benzing
44	0675239	J	Perno
45	0677012	P	Perno
46	6331110	N	Rondella Ø 10,5
47	6313106	M	Vite T.C.C.E. 3 x 20
48	0005331	U	Magnetino
49	6331103	A	Rondella piana Ø 3,2
50	7459203	N	Dado M3
51	7465706	V	Rondella piana Ø 4,3
52	0682871	D	Dado M4
53	6332104	B	Rondella elast. Ø 4,3
54	0675340	J	Supp. Cerniera
55	0675262	X	Vite Bloccaggio
56	6337107	L	Anello elastico
57	0815207	H	Pannello laterale
58	0675349	N	Piano di appoggio
59	6313147	H	Vite TC 6 x 12
60	0676333	E	Battuta di chiusura



1	0675349 M	Piano di appoggio con perno
2	0675273 U	Perno basso fissaggio piano di appoggio
	0675274 R	Perno alto fissaggio piano di appoggio
3	0817207 H	Pannelli laterali
4	0817158 M	Pannelli post. sinist. ed ant. destro
5	0817159 R	Pannelli post. destro ed ant. sinistro
6	0675339 L	Cerniera pannelli frontali
7	0005331 U	Piastrina per magnete
8	0675266 Y	Cerniera
9	0005331 U	Magnete
10	0675344 Q	Squadretta arresto profilo
11	0005338 S	Gommino paracolpi
12	0674048 Y	Molla per cerniera
13	0677012 P	Perno
14	6337114 V	Anello elastico
15	0836416 G	Cuneo superiore
16	0836415 Y	Cuneo in gomma
17	0836417 G	Tassello d'estremità
18	6337116 D	Anello elastico
19	0836413 E	Vite regolazione corsa cuneo
20	6313106 M	Vite TCE M3 x20
21	6332103 A	Rondella elastica Ø 3,2
22	7459203 N	Dado M3
23	6348324 G	Vite TC autofilettante 2,9 x 6,35
24	6313710 G	Vite TSCE M4 x10
25	6321104 W	Dado M4
26	6332104 B	Rondella elastica Ø 4,3
27	7465706 V	Rondella piana Ø 4,3
28	6313116 A	Vite TCE M4 x 12
29	6313148 W	Vite TCE M6 x 15
30	6331106 F	Rondella piana Ø 6,4
31	6321106 E	Dado M6
32	6337107 L	Anello elastico
33	0674050 S	Perno
34	6337106 Q	Anello seeger
35	0674954 J	Copertura laterale
36	0674956 S	Copertura ant. e post.
37	0677018 H	Gancio di arresto
38	0677257 B	Vite di perno
39	0675239 J	Perno
40	0676333 E	Battuta di chiusura
41	6313132 B	Vite TCCE 5x15
42	6331105 T	Rondella piana Ø 5,3
43	6332105 F	Rondella elastica Ø 5,3
44	6332106 K	Rondella elastica Ø 6,4
45	0676522 M	Gruppo profilo
46	0675262 X	Vite di bloccaggio
47	0675327 S	Parte esterna di cerniera
48	6348290 X	Vite autofilettante

Nota : I codici di questa pagina sono validi solo per DSC 161/162 fino alla matr. 0479. Per le matricole superiori e DSC 157 vedere pagina seguente.

Note : Part numbers shown on this page are only valid for the DSC 161/162 with S/N up to 0479. For those having S/N above 0479 and the DSC 157, refer to the following page.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1	0610089 C	Piastrina CONT 2B
2	0610090 A	Piastrina CONT 2C
3	0616028 G	Piastrina FLIT 2C
4	0616029 C	Piastrina FLIT 2E
5	0610091 B	Piastrina FLIC 2A
6	0610092 P	Piastrina FLIC 2B
7	0610093 K	Piastrina FLIC 2C
8	0610094 G	Piastrina FLIC 2D
9	0610095 C	Piastrina FLIP 2A
10	0610096 Q	Piastrina FLIP 2B
11	0610097 L	Piastrina FLIP 2C
12	0610098 H	Piastrina FLIP 2D
13	0610099 D	Piastrina FLIP 2E
14	0610220 N	Piastrina FLIP 2F
15	0610221 P	Piastrina FLIP 2G
16	0610100 W	Piastrina FLJK 2A
17	0610101 X	Piastrina FLIK 2B
18	0610027 D	Piastrina GEMA 2A
19	0610222 T	Piastrina INOR 2A
20	0610032 H	Piastrina INVE 2A
21	0610033 D	Piastrina LIRI 2A
22	0610123 V	Piastrina LIRI 2F
23	0610102 B	Piastrina LOCO 2A
24	0610196 H	Piastrina LOCO 2B
25	0610104 U	Piastrina LOCO 2C
26	0610105 Y	Piastrina LOCO 2D
27	0610106 C	Piastrina LOCO 2E
28	0610044 T	Piastrina LOSE 2G
29	0610107 G	Piastrina LOVA 2A
30	0610108 V	Piastrina LOVA 2B
31	0610109 Z	Piastrina LOVA 2C
32	0610053 V	Piastrina PATE 2A
33	0610085 B	Piastrina PHOS D
34	0619107 B	Piastrina RICO B
35	0610223 X	Piastrina RILE 2B
36	0610122 Z	Piastrina RIRA 2A
37	0610110 K	Piastrina RECO 2A
38	0610219 Q	Piastrina RECO 2B
39	0610111 L	Piastrina REDI 2B
40	0610112 Y	Piastrina REGI 2A
41	0610113 V	Piastrina REGI 2B
42	0610115 M	Piastrina SHIF 2A
43	0610116 Z	Piastrina SHSI 2A
44	0619106 F	Piastrina TACO
45	0610118 J	Piastrina TAPO 2A
46	0610224 L	Piastrina TASE 2B
47	0610088 G	Piastrina TERE 2A
48	0610120 L	Piastrina TRIN 2B
49	0610119 N	Piastrina TRAN 2A
* 50	0610121 M	Piastrina UNI 32A
51	0842831 J	GR. tarato LIRI 2A - SPIL 2A
52	0842832 W	GR. tarato RIRI 2A - PHOS D

Nota : Per i componenti delle piastrine consultare la documentazione di macchina al Vol. 8F.

Note : For PWB component details, refer to the Machine documentation Vol. 8F

* **Nota** : Prima del montaggio consultare la "Distinta Tempi Univibratori" dis. 78B103849. Vol. 7

* **Note** : Before mounting, consult the One-shot Timing Chart on Dwg. 78B103849. Vol. 7

1	0610089 C	PST CONT 2B
2	0610090 A	PST CONT 2C
3	0616028 G	PST FILT 2D
4	0616029 C	PST FILT 2E
5	0610091 B	PST FLIC 2A
6	0610092 P	PST FLIC 2B
7	0610093 K	PST FLIC 2C
8	0610094 G	PST FLIC 2D
9	0610095 C	PST FLIP 2A
10	0610096 Q	PST FLIP 2B
11	0610097 L	PST FLIP 2C
12	0610098 H	PST FLIP 2D
13	0610099 D	PST FLIP 2E
14	0610100 W	PST FLJK 2A
15	0610101 X	PST FLJK 2B
16	0610027 D	PST GEMA 2A
17	0610032 H	PST INVE 2A
18	0610102 B	PST LOCO 2A
19	0610196 H	PST LOCO 2B
20	0610104 U	PST LOCO 2C
21	0610105 Y	PST LOCO 2D
22	0610106 C	PST LOCO 2E
23	0610044 T	PST LOSE 2G
24	0610107 G	PST LOVA 2A
25	0610108 V	PST LOVA 2B
26	0610109 Z	PST LOVA 2C
27	0610033 D	PST LIRI 2A
28	0610123 V	PST LIRI 2F
29	0610053 F	PST PATE 2A
30	0610085 B	PST PHOS D
31	0610110 K	PST RECO 2A
32	0610111 L	PST REDI 2B
33	0610112 Y	PST REGI 2A
34	0610113 V	PST REGI 2B
35	0619107 B	PST RICO B
36	0610087 K	PST RILE 2A
37	0610122 Z	PST RIRA 2A
38	0610114 R	PST RIRI 2A
39	0610115 M	PST SHIF 2A
40	0610116 Z	PST SHSI 2A
41	0610117 V	PST SPIL 2A
42	0619106 F	PST TACO
43	0610118 J	PST TAPO 2A
44	0610086 P	PST TASE
45	0610088 G	PST TERE 2A
46	0610119 N	PST TRAN 2A
47	0610120 L	PST TRIN 2B
*48	0610121 M	PST UNI 3 2A
49	0842831 J	GR. tarato LIRI 2A - SPIL 2A
50	0842832 W	GR. tarato RIRI 2A - PHOS D
51	0610232 U	PST LIMI 2 A (Solo per DSC 150)

Nota : Per i componenti delle piastrine consultare la documentazione di macchina al Vol. 8F

Note : For PWB component details, refer to the Machine documentation Vol. 8F

* **Nota** : Prima del montaggio consultare la "Distinta Tempi Univibratori" dis. 78B103849. Vol. 7

* **Note** : Before mounting, consult the One-shot Timing Chart on Dwg. 78B103849. Vol. 7

REPERTORIO NUMERICO

Codice	Pag.	Rif.
0000867H	28	8
0000883J	20	71
0000885B	28	43
0000887K	28	44
0001123E	26	23
0001124T	26	22
0001218Y	30	14
0001231Z	26	24
0001234X	4	8
0001234X	8	8
0001238X	4	45
0001238X	8	45
0001238X	18	25
0001238X	30	13
0001244X	30	15
0001254Y	4	46
0001254Y	8	46
0001254Y	18	26
0001258Z	4	46
0001258Z	8	46
0001265V	4	46
0001265V	8	46
0001307L	16	12
0001307L	18	3
0001309D	18	2
0001315S	30	5
0001354S	30	6
0001355W	30	3
0001370W	18	15
0001373F	30	7
0001375Y	4	23
0001375Y	8	23
0001386H	18	22
0001402S	4	10
0001402S	8	10
0001402S	16	48
0001402S	18	6
0001403W	4	32
0001403W	12	20
0001426R	26	19
0001434A	14	31
0001449G	30	1
0001481J	28	3
0001482W	12	48
0001506Y	14	47
0001506V	18	10
0001506V	20	68
0001614C	6	77

Codice	Pag.	Rif.
0001614C	12	1
0001614C	28	1
0001692J	20	51
0001699R	26	21
0001700K	26	20
0001710A	4	22
0001710A	8	22
0001710A	16	44
0001821V	30	2
0001822H	30	2
0001858W	6	60
0001858W	10	60
0001858W	12	17
0001858W	20	65
0001858W	28	42
0001875T	30	8
0001876F	6	74
0001876F	28	32
0001884G	30	4
0001885C	30	4
0002118F	18	8
0002138H	4	9
0002138H	8	9
0005331U	32	7
0005331U	32	9
0005331U	34	9
0005331U	36	48
0005338S	32	11
0005338S	34	18
0610027D	38	18
0610027D	39	16
0610032H	38	20
0610032H	39	17
0610033D	38	21
0610033D	39	27
0610044T	38	28
0610044T	39	23
0610053V	38	32
0610053F	39	29
0610085B	38	33
0610085B	39	30
0610086P	39	44
0610087K	39	36
0610088G	38	47
0610088G	39	45
0610089C	38	1
0610089C	39	1
0610090A	38	2

Codice	Pag.	Rif.
0610090A	39	2
0610091B	38	5
0610091B	39	5
0610092P	38	6
0610092P	39	6
0610093K	38	7
0610093K	39	7
0610094G	38	8
0610094G	39	8
0610095C	38	9
0610095C	39	9
0610096Q	38	10
0610096Q	39	10
0610097L	38	11
0610097L	39	11
0610098H	38	12
0610098H	39	12
0610099D	38	13
0610099D	39	13
0610100W	38	16
0610100W	39	14
0610101X	38	17
0610101X	39	15
0610102B	38	23
0610102B	39	18
0610104U	38	25
0610104U	39	20
0610105Y	38	26
0610105Y	39	21
0610106C	38	27
0610106C	39	22
0610107G	38	29
0610107G	39	24
0610108V	38	30
0610108V	39	25
0610109Z	38	31
0610109Z	39	26
0610110K	38	37
0610110K	39	31
0610111L	38	39
0610111L	39	32
0610112Y	38	40
0610112Y	39	33
0610113V	38	41
0610113V	39	34
0610114R	39	38
0610115M	38	42
0610115M	39	39

Codice	Pag.	Rif.
0610116Z	38	43
0610116Z	39	40
0610117V	39	41
0610118J	38	45
0610118J	39	43
0610119N	38	49
0610119N	39	46
0610120L	38	48
0610120L	39	47
0610121M	38	50
0610121M	39	48
0610122Z	38	36
0610122Z	39	37
0610123V	38	22
0610123V	39	28
0610196H	38	24
0610196H	39	19
0610219Q	38	38
0610220N	38	14
0610221P	38	15
0610222T	38	19
0610223X	38	35
0610224L	38	46
0610232U	41	51
0616028G	38	3
0616028G	39	3
0616029C	38	4
0616029C	39	4
0619106F	38	44
0619106F	39	42
0619107B	38	34
0619107B	39	35
0620104V	6	65
0620104V	10	65
0620111M	18	30
0620112Z	14	AP
0620113V	20	69
0620114J	4	29
0620114J	8	29
0620115N	14	46
0620116S	14	48
0620229J	10	66
0620231R	16	21
0620233Z	4	17
0620233Z	8	17
0620233Z	20	49
0620234N	16	18
0620239K	4	30

Codice	Pag.	Rif.
0620239K	8	30
0620240R	16	22
0620243S	16	20
0643358W	22	AG
0674048Y	32	12
0674048Y	34	16
0674050S	32	33
0674050S	34	20
0674139L	28	18
0674141K	28	21
0674142X	28	23
0674143T	28	20
0674145L	28	22
0674146Y	28	26
0674149M	28	25
0674159N	28	16
0674501B	28	19
0674502P	28	24
0674543B	26	62
0674593Q	34	AG
0674943U	34	31
0674944R	34	32
0674953V	34	2
0674954J	32	35
0674956S	32	36
0674965N	34	1
0675226U	26	63
0675239J	32	39
0675239J	36	44
0675262X	32	46
0675262X	36	55
0675266Y	32	8
0675266Y	34	11
0675273U	32	2
0675274R	32	2
0675318N	34	4
0675323Z	34	14
0675327S	32	47
0675327S	34	17
0675339L	32	6
0675340J	36	54
0675344Q	32	10
0675349M	32	1
0675349N	36	58
0676291A	36	38
0676292N	36	36
0676294F	36	37
0676295B	36	AG

Codice	Pag.	Rif.
0676296P	36	35
0676333E	32	40
0676333E	36	60
0676522M	32	45
0676522H	34	15
0676526N	34	7
0676527J	34	13
0676528F	34	6
0676529B	34	5
0676530H	34	12
0676535B	34	AP
0676539C	34	AG
0676540A	34	AG
0677012P	32	13
0677012P	36	45
0677018H	32	37
0677018H	36	41
0677257B	32	38
0677257B	36	42
0680116G	14	44
0680116G	16	57
0680311X	26	53
0680490Q	12	30
0680541E	26	52
0680550G	16	46
0680550E	26	44
0682260E	16	45
0682260E	26	47
0682456X	12	32
0682456X	16	47
0682456X	26	45
0682560L	26	55
0682865D	28	14
0682871D	36	52
0683040M	16	58
0683086F	12	31
0683086F	24	20
0683086F	26	46
0683131E	26	54
0683542T	28	15
0815207H	36	57
0817158N	32	4
0817159R	32	5
0817207H	32	3
0818240C	6	AP
0818241D	6	AG
0818242R	4	27
0818243M	4	28

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Codice	Pag.	Rif.
0818247N	4	26
0819107X	22	13
0819108M	22	12
0819109R	22	19
0819110B	22	5
0819112Q	22	6
0819113L	22	7
0819114H	22	8
0819115D	22	9
0819117M	22	1
0819150F	6	68
0819293W	6	67
0819299Q	6	66
0819300J	6	73
0819303T	6	71
0819304Q	6	70
0819307U	6	72
0819342P	6	79
0830388L	4	35
0830388L	8	35
0830388L	12	16
0830388L	20	50
0830396U	20	72
0830512X	12	2
0830512X	16	29
0830662W	12	AG
0833359N	4	42
0833359N	8	42
0834000S	26	1
0834007C	26	57
0834008Z	26	56
0834009V	26	58
0834139J	26	33
0834661Q	6	47
0834661Q	10	47
0834661Q	12	50
0834661Q	20	48
0834661Q	26	60
0834662U	4	39
0834662U	8	39
0834662U	12	41
0834662U	20	47
0834662X	26	13
0834663Y	4	40
0834663Y	8	40
0834663Y	12	42
0834663Y	26	15
0834665R	6	48

Codice	Pag.	Rif.
0834665R	10	48
0834665R	12	49
0834665R	26	61
0835132K	12	43
0835132C	26	14
0835484X	12	AP
0836264M	26	AG
0836282E	26	59
0836413E	32	19
0836415Y	32	16
0836416G	32	15
0836417G	32	17
0836503L	12	45
0836507M	12	AG
0836508A	12	44
0836820Q	14	45
0836821R	6	62
0836821R	10	62
0836823Z	20	66
0836824N	20	54
0836825J	18	21
0836826M	20	52
0836848R	28	40
0836871R	12	47
0836940L	26	66
0836945N	6	61
0836945N	10	61
0836946S	20	67
0837160R	16	60
0837214L	4	43
0837214L	8	43
0837215Q	28	17
0837218M	4	18
0837218M	8	18
0837218M	18	5
0837237S	24	7
0837238P	24	10
0837239K	24	8
0837241J	24	9
0837242W	24	1
0837243S	24	6
0837244P	22	11
0837244P	24	12
0837245K	24	5
0837246X	22	10
0837246X	24	4
0837247T	24	11
0837249L	26	5

Codice	Pag.	Rif.
0837250J	26	6
0837251K	26	3
0837252X	26	2
0837254Q	26	7
0837255L	26	8
0837256Y	26	4
0837257U	26	30
0837258R	26	29
0837259M	26	26
0837262Y	26	43
0837275N	30	12
0837277W	30	10
0837318P	20	62
0837380X	18	28
0837519X	14	18
0837519E	16	59
0837630Y	18	1
0837633H	18	9
0837634R	20	46
0837641S	20	61
0837644X	8	34
0837652F	12	19
0837657C	14	7
0837659U	14	25
0837664Z	28	10
0837668S	26	28
0837671V	26	31
0837678T	12	15
0837679K	12	13
0837679K	14	35
0837742G	26	27
0837753D	26	9
0837919Q	14	11
0837927J	14	4
0837927J	16	36
0837928M	16	41
0837931Q	14	36
0837931Q	16	28
0837933Y	12	9
0837934M	12	7
0837937Z	14	1
0837937Z	16	23
0837952W	14	10
0837956X	16	24
0837988T	18	29
0838039M	26	16
0838137M	4	31
0838137M	8	31

Codice	Pag.	Rif.
0838137M	14	5
0838137M	16	40
0838137M	18	27
0838276P	14	6
0838682F	14	32
0838723X	28	36
0838961G	4	44
0838961G	8	44
0839117P	18	44
0839264A	18	39
0839266J	4	33
0839266J	12	18
0839267N	8	36
0839336R	6	76
0839344A	4	13
0839344A	8	13
0839348B	4	14
0839348B	8	14
0839352Y	4	34
0839353N	4	15
0839353N	8	15
0839356K	8	32
0839356K	28	4
0839359G	20	53
0839360E	4	12
0839360E	8	12
0839367Q	4	11
0839367Q	8	11
0839377R	4	36
0839377R	12	22
0839418J	4	38
0839418J	8	38
0839418J	20	44
0839420L	4	41
0839420L	8	41
0839421M	4	37
0839421M	8	37
0839473S	26	12
0839474P	26	11
0839652Y	12	21
0839653U	4	16
0839653U	8	16
0839653U	18	42
0839653O	28	6
0839772W	26	10
0842490E	26	18
0842491F	26	17
0842532F	16	AG

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Codice	Pag.	Rif.
0842609G	28	AG
0842616G	12	14
0842626H	14	17
0842632H	14	AG
0842634S	16	AG
0842635W	16	AG
0842638T	28	12
0842650A	4	21
0842650A	8	21
0842651X	8	28
0842652B	8	27
0842653F	8	26
0842780B	4	24
0842780B	8	24
0842781A	4	25
0842781A	8	25
0842808Z	26	25
0842831J	38	51
0842831J	39	49
0842832W	38	52
0842832W	39	50
0842893G	16	1
3361200Z	6	AP
3543104P	12	23
3543104P	28	5
4934527T	4	19
4934527T	8	19
4934926Q	4	20
4934926Q	8	20
4962961R	28	11
4970085W	14	29
4971060K	14	26
4971065M	14	28
4971086B	16	16
4971086B	16	17
4972832Z	18	14
4972956W	20	70
4973077E	18	7
4973230K	18	13
4973235M	18	17
4973450Z	18	19
4973474Z	16	15
4973600C	18	12
4973633C	18	11
4973636H	18	18
4973761Z	18	16
4973798A	18	20
4974076X	14	27

Codice	Pag.	Rif.
4979005V	20	74
4991070W	16	3
4991070W	16	4
4991248M	14	21
4991270R	14	22
4991415Z	16	7
4993305A	16	5
4993305A	16	6
4993540C	16	2
4999530V	14	19
4999530V	16	9
4999550X	14	20
4999550X	16	8
5032090G	14	30
5035679S	16	13
5035679S	16	14
5035825Q	4	7
5035825Q	8	7
5038680C	4	6
5038680C	8	6
5041355Q	16	19
5041455S	16	19
5045270P	18	4
5045550T	4	5
5045550T	8	5
5104015H	20	60
5141133J	14	9
5141133N	16	35
5241302W	14	3
5241302W	16	39
5268012Y	14	33
5268016W	14	34
5268050L	12	40
5268052Z	12	11
5268060M	12	12
5326600B	18	23
5326620Z	20	73
5361011M	20	58
5363150R	20	59
5363152W	20	57
5363153S	20	55
5363154P	20	56
5373100Z	12	25
5373104X	12	24
5373106F	12	39
5421000E	16	26
5421000E	16	27
5421004B	16	25

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Codice	Pag.	Rif.
5421007P	8	1
5427065A	18	24
5445093T	4	4
5445093T	8	4
5445095F	4	2
5445095F	8	2
5445098C	4	3
5445098C	8	3
5541340N	6	78
5541340N	12	37
5541340N	28	2
5610021W	14	23
5610021W	16	10
5610022Q	24	3
5610024T	14	24
5610024J	16	11
5612447M	30	11
5612453M	6	75
5612540D	8	33
5612540D	28	7
5612595K	30	9
5613858Y	28	9
5613860S	28	41
7465706V	36	51
5616020B	22	20
5616020B	24	2
5616022Q	22	18
5616413J	14	13
5616413J	16	34
5616415B	12	3
5616418G	14	12
5616418G	16	30
5616450D	14	14
5616450D	16	31
5616452J	14	15
5616452J	16	32
5616454B	14	16
5616454B	16	33
5616455F	12	4
5616457P	12	5
5616459G	12	6
5618052C	28	34
5618054V	26	32
5621016G	4	1
5812010W	16	42
5812012B	16	43
5826513A	20	64
5826515T	14	8

Codice	Pag.	Rif.
5826515T	20	63
5836000C	16	38
5836002R	14	2
5836002R	16	37
6307430Q	26	34
6311203Q	14	41
6311230Q	6	69
6311230Q	16	52
6311230Q	18	33
6311231R	6	49
6311231R	10	49
6311231R	12	28
6311231R	18	31
6311231R	26	48
6311231R	28	39
6311232V	22	21
6311232V	24	16
6311232V	26	37
6311233Z	16	54
6311234N	6	56
6311234N	10	56
6311234N	12	26
6311234N	14	43
6311234N	18	38
6311234N	22	14
6311234N	24	13
6311234N	26	51
6311234N	30	19
6311236W	12	38
6311236W	24	17
6311236W	26	50
6311242W	6	58
6311242W	10	58
6311242W	18	35
6311242W	22	17
6311242W	24	19
6311242W	28	30
6311243S	16	56
6311243S	22	2
6311243S	30	18
6311244P	26	42
6311245K	6	53
6311245K	10	53
6311245K	12	33
6311245K	18	40
6311245K	30	17
6311247T	26	38
6311247J	28	38

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Codice	Pag.	Rif.
6311258R	6	63
6311258R	10	63
6311931B	14	42
6312725F	28	13
6312732R	16	53
6312736L	12	36
6312743Q	24	21
6313102L	28	29
6313106M	32	20
6313106M	36	47
6313113D	14	37
6313113D	18	34
6313116A	32	28
6313116A	34	27
6313132B	32	41
6313132B	34	23
6313147H	36	59
6313148W	32	29
6313148W	34	28
6313710G	32	24
6313710G	34	8
6321103H	6	57
6321103H	10	57
6321103H	12	35
6321103H	14	39
6321103H	16	49
6321103H	20	43
6321103M	22	22
6321103H	24	18
6321103H	26	36
6321103H	28	33
6321104W	26	41
6321104W	30	21
6321104W	32	25
6321105S	26	65
6321105S	28	28
6321106E	32	31
6321106E	34	26
6321120N	34	34
6331103A	6	51
6331103A	10	51
6331103A	12	27
6331103A	14	40
6331103A	16	51
6331103A	18	32
6331103A	22	15
6331103A	24	15
6331103N	26	35

Codice	Pag.	Rif.
6331103A	26	49
6331103A	28	37
6331103A	36	49
6331104X	6	55
6331104X	10	55
6331104X	12	46
6331104X	18	36
6331104X	22	4
6331104X	26	39
6331104X	30	22
6331105T	6	59
6331105T	10	59
6331105T	28	27
6331105T	32	42
6331105T	34	24
6331106F	32	30
6331106F	34	29
6331108Y	12	8
6331110N	36	46
6332103N	6	50
6332103N	10	50
6332103N	12	29
6332103N	14	38
6332103N	16	50
6332103N	18	37
6332103N	22	16
6332103N	24	14
6332103A	32	21
6332104B	6	54
6332104B	10	54
6332104B	12	34
6332104B	16	55
6332104B	18	41
6332104B	22	3
6332104X	26	40
6332104B	28	31
6332104B	32	26
6332104B	36	53
6332105S	6	64
6332105S	10	64
6332105F	26	64
6332105F	32	43
6332105F	34	25
6332106K	32	44
6332106K	34	30
6332303J	30	20
6332304F	30	16
6337105Q	6	52

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6337106Q	20	45
6337106Q	32	34
6337106Q	34	19
6337107L	32	32
6337107L	36	56
6337112C	36	40
6337114V	32	14
6337114V	36	43
6337116D	32	18
6337120Y	34	33
6343048G	12	10
6348290X	32	48
6348290X	34	10
6348324G	32	23
6348324G	34	3
6371522G	36	39
6476416X	34	21
6476420S	34	22
7454750B	28	35
7459203N	32	22
7459203N	36	50
7465706V	32	27
9940338D	18	43

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